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CAD Note:

Default component footprint is SMD 0201, X5R, 1% resistors.

Property: BUILD-OPT  
DNP = Do Not Populate

DBG\_S - Replace with board short for MP  
DBG\_R - Replace with lower cost component for MP  
DBG\_N - Install for Non-Debug Builds  
DBG\_D - Remove from BOM (Depopulate) for MP  
DBG\_T - Used for Telemetry in MP as needed  
DBG\_TS - Used for Telemetry in MP as needed. This part needs to be replaced with a short if telemetry is not needed.

<Variant Name>

## SchematicsChangeHistory

[illegible]

## CAD Note:

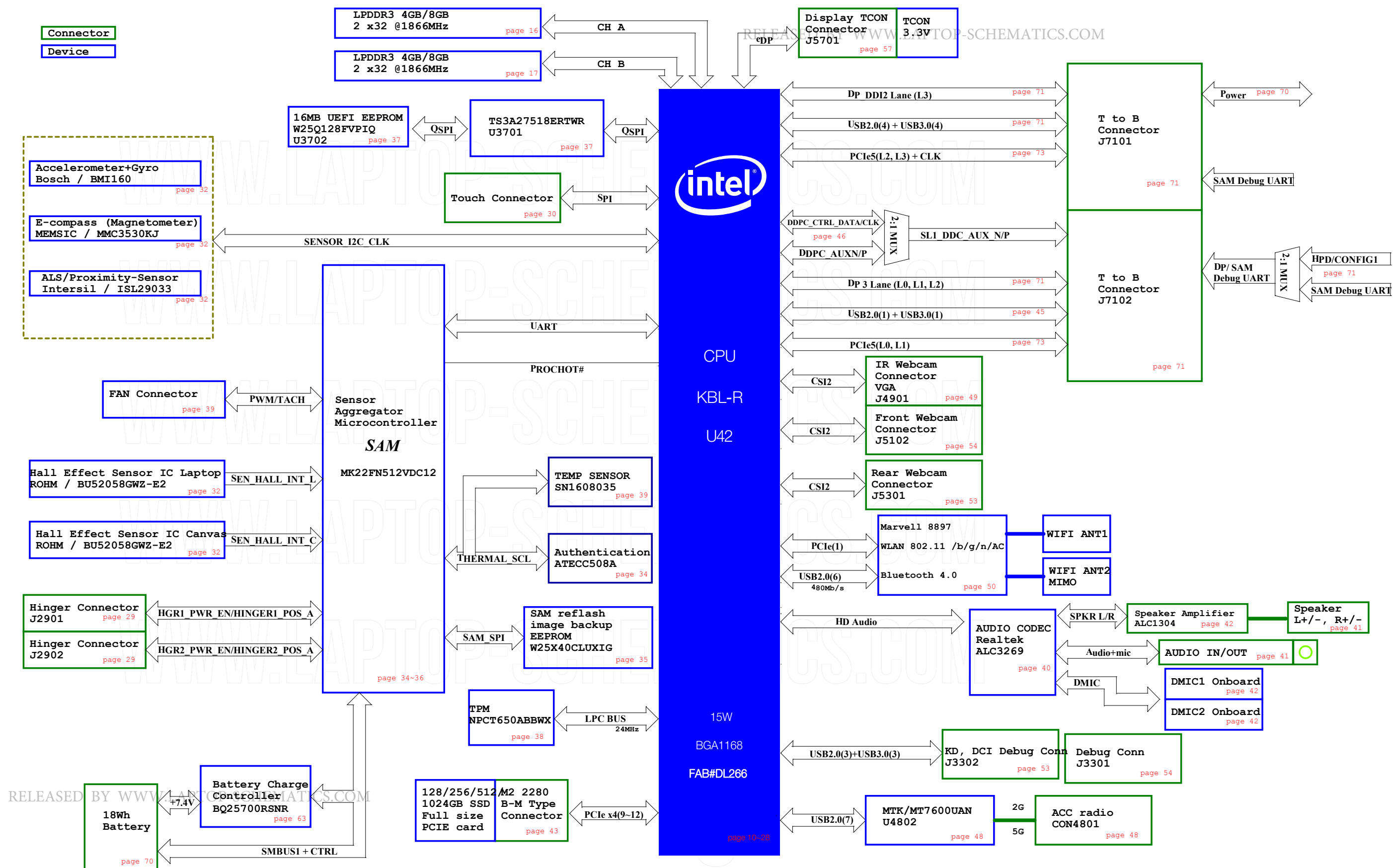
Default component footprint is  
SMD 0201, X5R, 1% resistors.

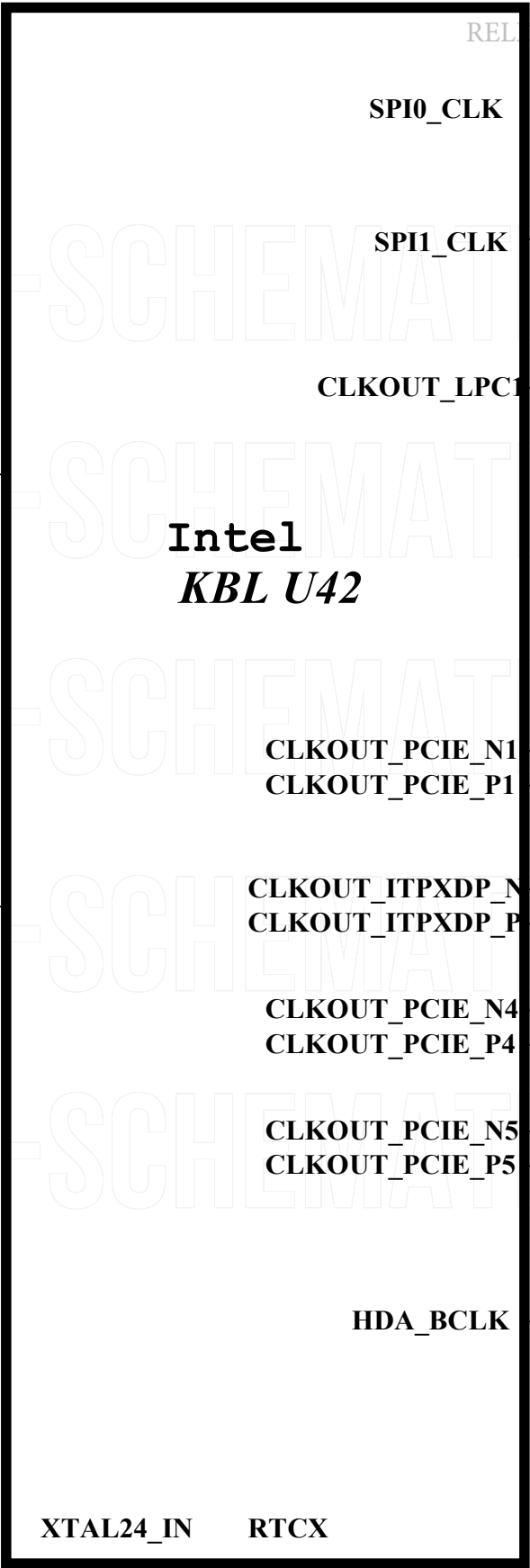
Property: BUILD-OPT  
DNP = Do Not Populate

```
DBG_S - Replace with board short for MP
DBG_R - Replace with lower cost component for MP
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DBG_T - Used for Telemetry in MP as needed
DBG_TS - Used for Telemetry in MP as needed. This part
needs to be replaced with a short if telemetry is not
```

### <Core Design>

\_\_\_\_\_





M\_CHA\_CLK[0..1]/#

M\_CHB\_CLK[0..1]/#

SPI0\_CLK

SPI\_CLK  
50 MHz

*SPI ROM*

SPI1\_CLK

TS\_SPI\_CLK\_1V8

*TOUCH*

CLKOUT\_LPC1

CK\_24M\_TPM  
24 MHz

*TPM*

CLKOUT\_PCIE\_N1  
CLKOUT\_PCIE\_P1

PCIECLK\_SSD\_N  
PCIECLK\_SSD\_P  
100 MHz

*SSD*

CLKOUT\_ITPXD\_P\_N  
CLKOUT\_ITPXD\_P\_P

CLK\_XDP\_N  
CLK\_XDP\_P  
100 MHz

*XDP*

CLKOUT\_PCIE\_N4  
CLKOUT\_PCIE\_P4

PCIE\_GPU\_RCLK\_N  
PCIE\_GPU\_RCLK\_P  
100 MHz

*GPU*

CLKOUT\_PCIE\_N5  
CLKOUT\_PCIE\_P5

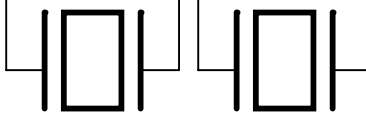
PCIE\_WIFI\_RCLK\_N  
PCIE\_WIFI\_RCLK\_P  
100 MHz

*WIFI*

HDA\_BCLK

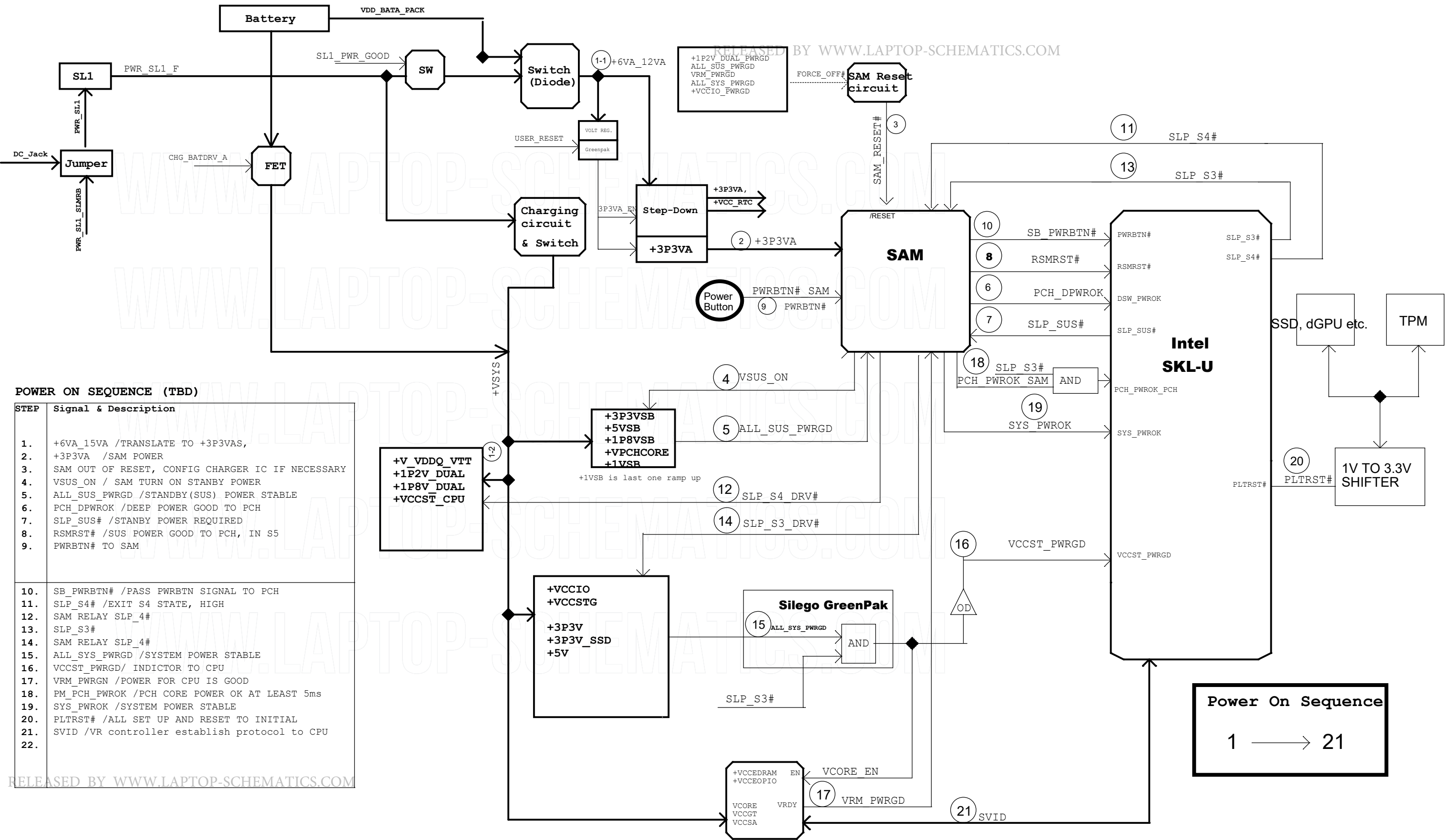
AZ\_BITCLK\_1  
24 MHz

*AUDIO CODEC*



<Core Design>







	15W SOC (CPU SKYLAKE-U)	
+VCORE	-> 29A	
+VCCGT	-> 56A	(GT2e)
	-> 62A	(GT3e)
+VCCSA	-> 5. 1A	
+VCCIO	-> 3. 1A	
+VCCEDRAM	-> 3A	(GT3e)
+VCCEOPIO	-> 3A	(GT3e)
+VCCST_CPU	-> 0. 24A	
+VCCPLL_OC	-> 0. 26A	
+DDR_V (+1P2V_DUAL)	-> 2A	
	(PCH)	
+VCCST	-> 0. 04A	
+VCCSTG	-> 0. 04A	
+1V_MODPHY	-> 2. 766A	
+1VSB	-> 0. 782A	
+VPCHCORE	-> 3A	
+1P8VSB	-> 0. 5A	
+3P3VSB	-> 0. 6A	

	LPDDR3	
+1P8V_DUAL	-> 0. 717A	
+1P2V_DUAL	-> 3. 5A	
+V_VDDQ_VTT (0.6V)	-> 1A	

	SSD (PCIe/mSATA)	
+3P3V	-> 2. 5A	

	EC	
+3P3V_EC	-> 0. 0375A	

	EC ROM	
+3P3V_EC	-> 0. 015A	

	Temp sensor (STTS751)	
+3P3V_EC	-> 0. 0005A (2PCS)	

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+3P3V_TPM (+3P3V)	TPM(Infineon SLB9665 ESS2)	
	-> 0. 1A	

	WiFi&BT	
+3P3V_WWAN	-> 1. 5A	

	DMIC	
DMIC_+3P3V/+3P3V_AUDIO	-> 0. 02A	

	FAN	
+5V_FAN	-> 0. 7A	

	UEFI_SPI_BIOS_ROM	
+3P3V	-> 0. 04A	

	Panel	
VCC_EDP_BKLT_IN	-> 0. 12A (30V)	
+3P3V_PANEL	-> 1. 5A	

	Touch Interface	
+1P8V_TS	-> 0. 452A	
+5V_TS	-> 0. 22A	

	ALC298 CODEC	
+5V_AUDIO	-> 1. 05A	
+1P8V_AUDIO	-> 0. 4A	

	DSP ALC5677	
+1P8V_AUDIO	-> 0. 1A	

	Camera REAR	
+1P2V_CAM_R	-> 0. 2A	
+1P8V_CAM_R	-> 0. 001A	
+2P8V_CAM_R	-> 0. 048A	
+3P3V_VCM	-> 0. 125A	
+3P3V (LED)	-> 0. 005A	
	Camera FRONT	
+1P8V_CAM_F	-> 0. 096A	
+2P8V_CAM_F	-> 0. 06A	
+3P3V (LED)	-> 0. 008A	

+3P3VA	Sensor uC (MKL17Z256VMP4)	
	-> 0. 001A	

	SL1	
+3P3V_HPD	->0. 075A	

	ACT_BOARD	
+3P3VSB	->2A (LEFT+RIGHT)	

	Hall effect sensor (BU52058GW-E2)	
+3P3VA	->0. 0028A	

	Compass (MMC3416XMA)	
+3P3V_SENSOR	->0. 0012A	

	Acceleromte&Gyro (BMI160)	
+3P3V_SENSOR	-> 0. 001A	

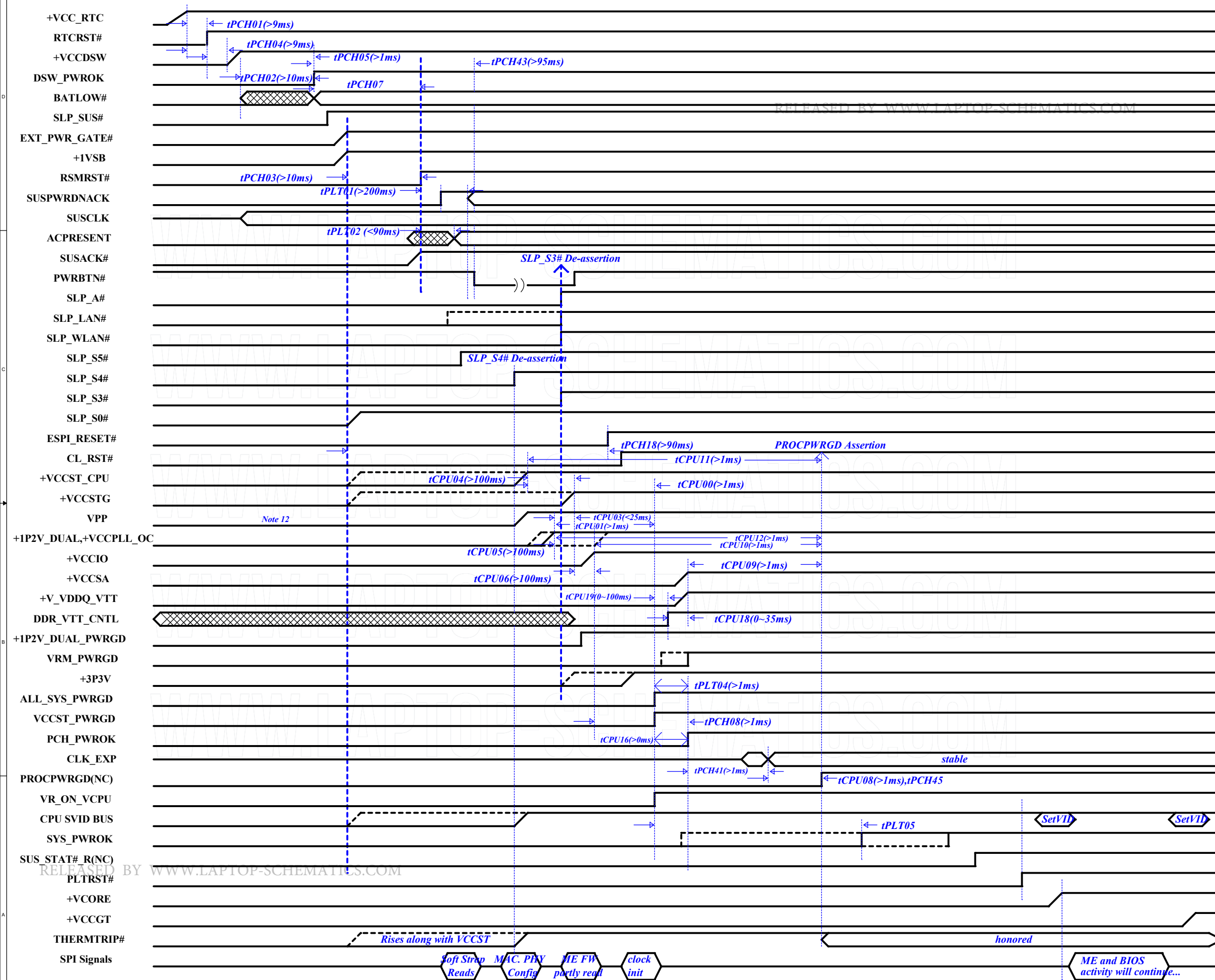
	ALS (ISL29033IROZ-T7)	
+3P3V_SENSOR	-> 0. 000075A	

	MUX	
+3P3V_MUX	-> 0. 0033A	

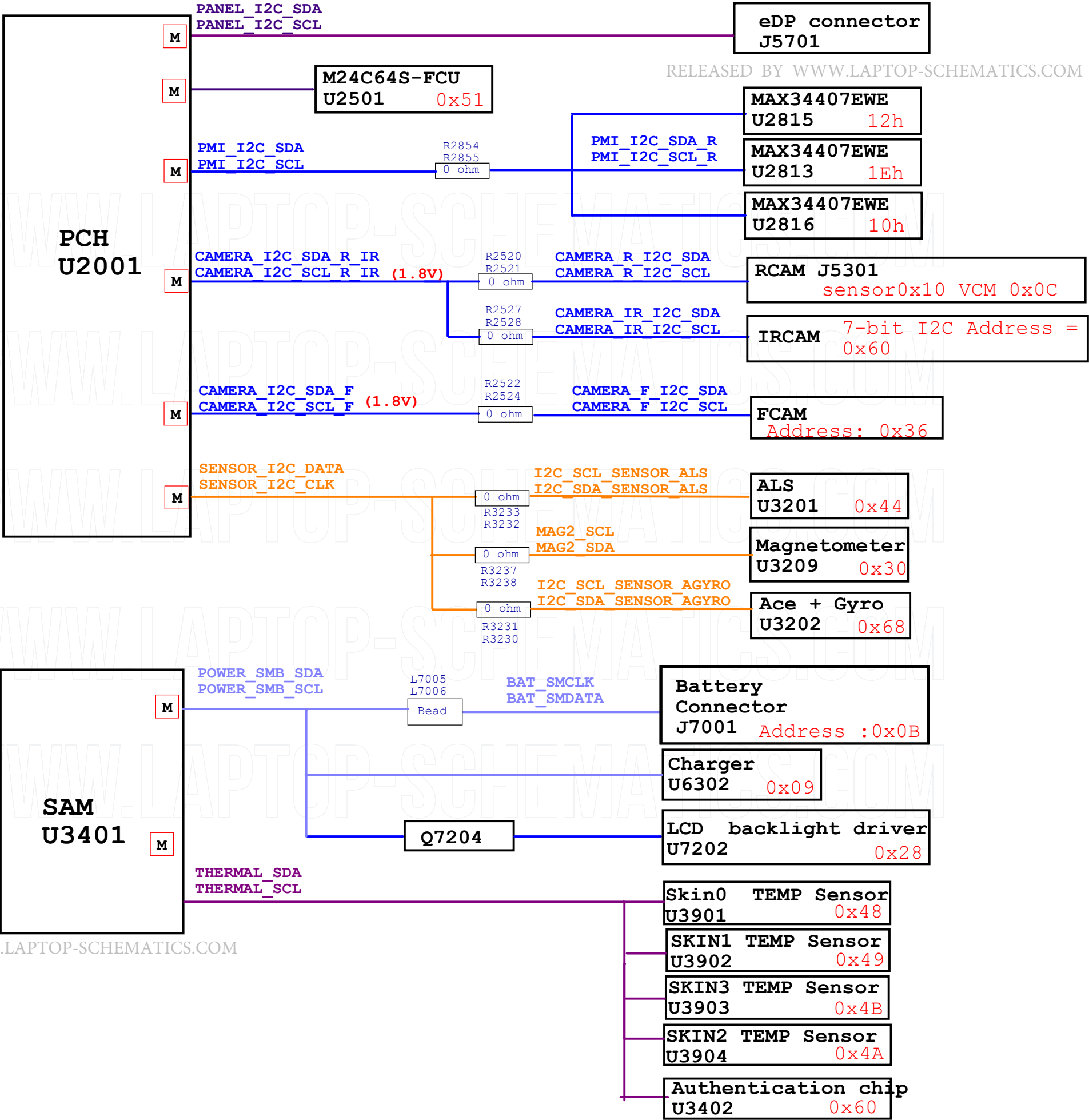
	mini DP	
+3P3V	-> 0. 5A	

	Battery Charger BQ24735	
+6VA_12VA	-> 0. 003A	

	Authentication IC (ECC108)	
+3P3VA	-> 0. 005A	

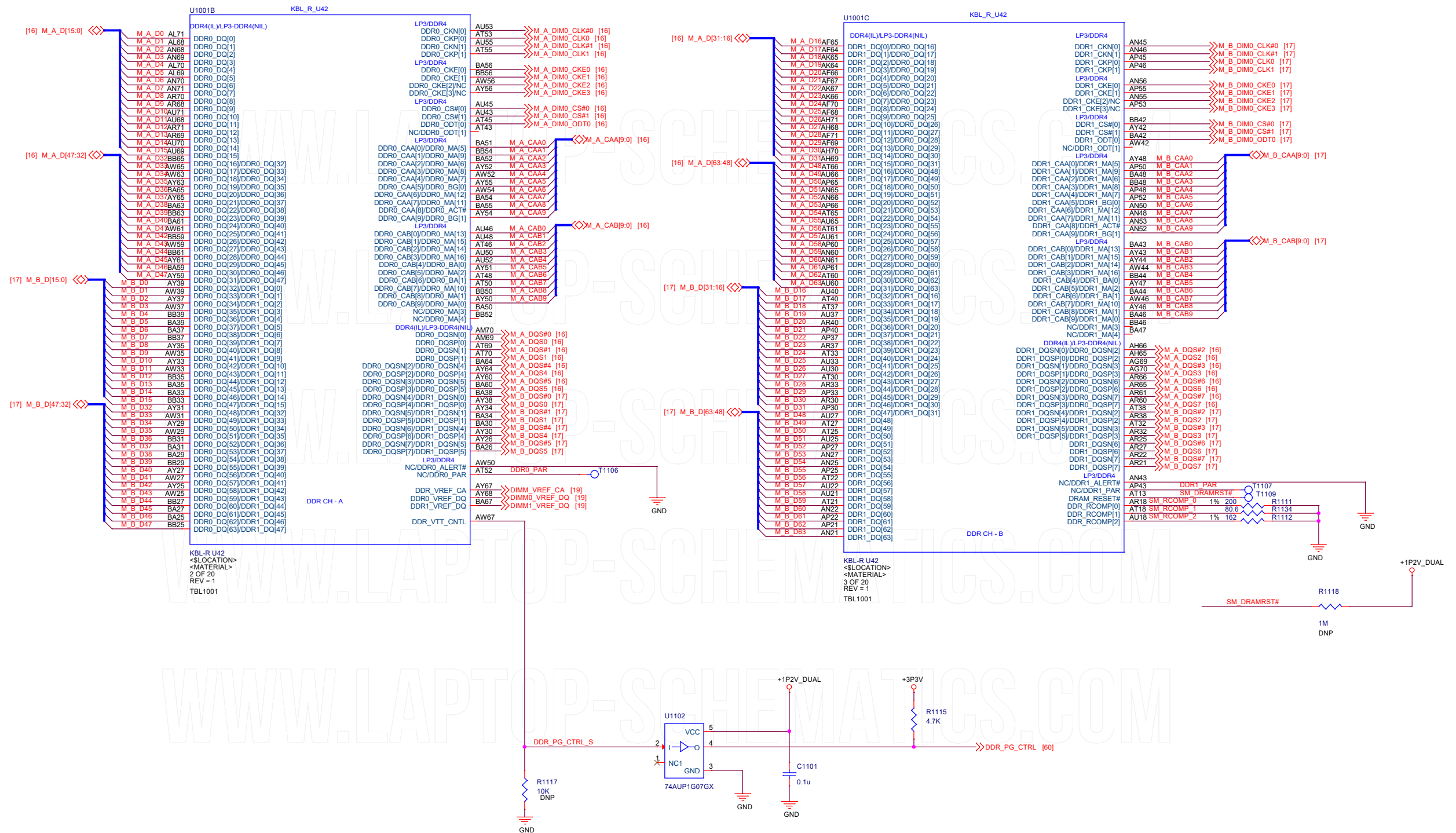


I2C & SMBUS Map

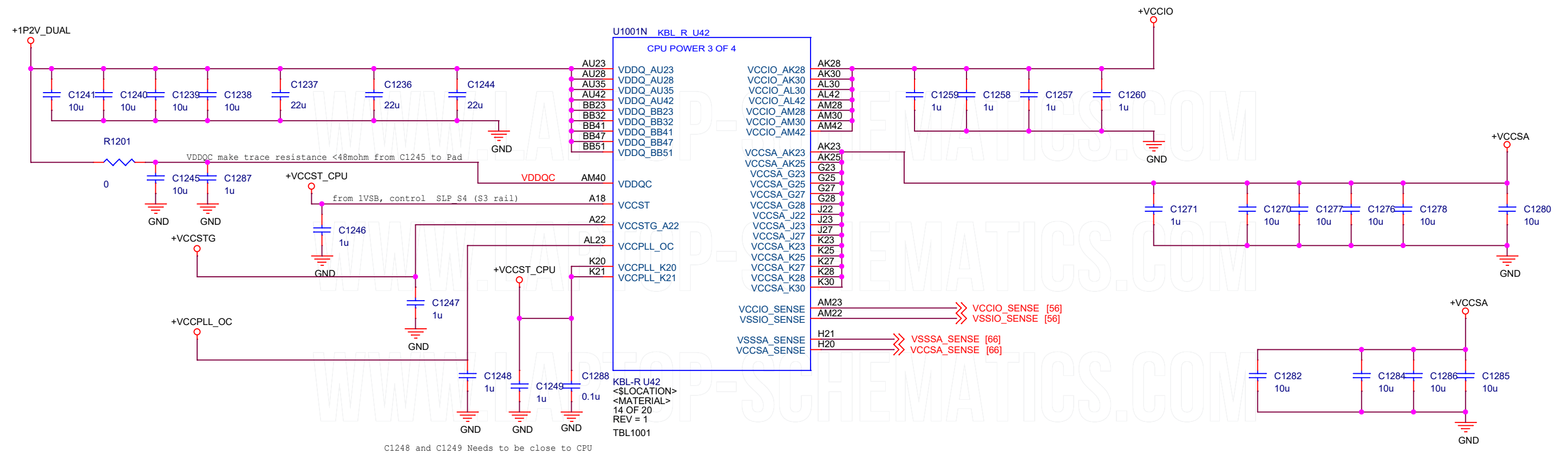




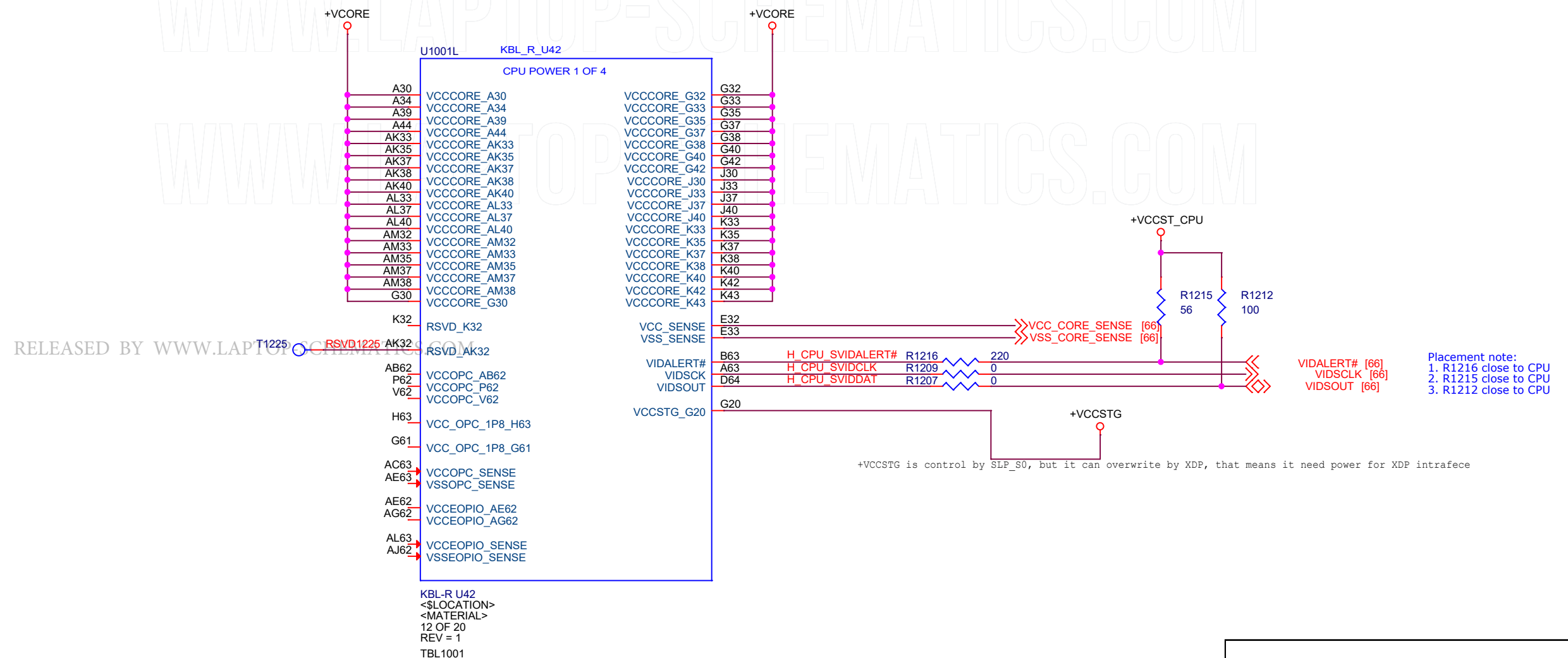


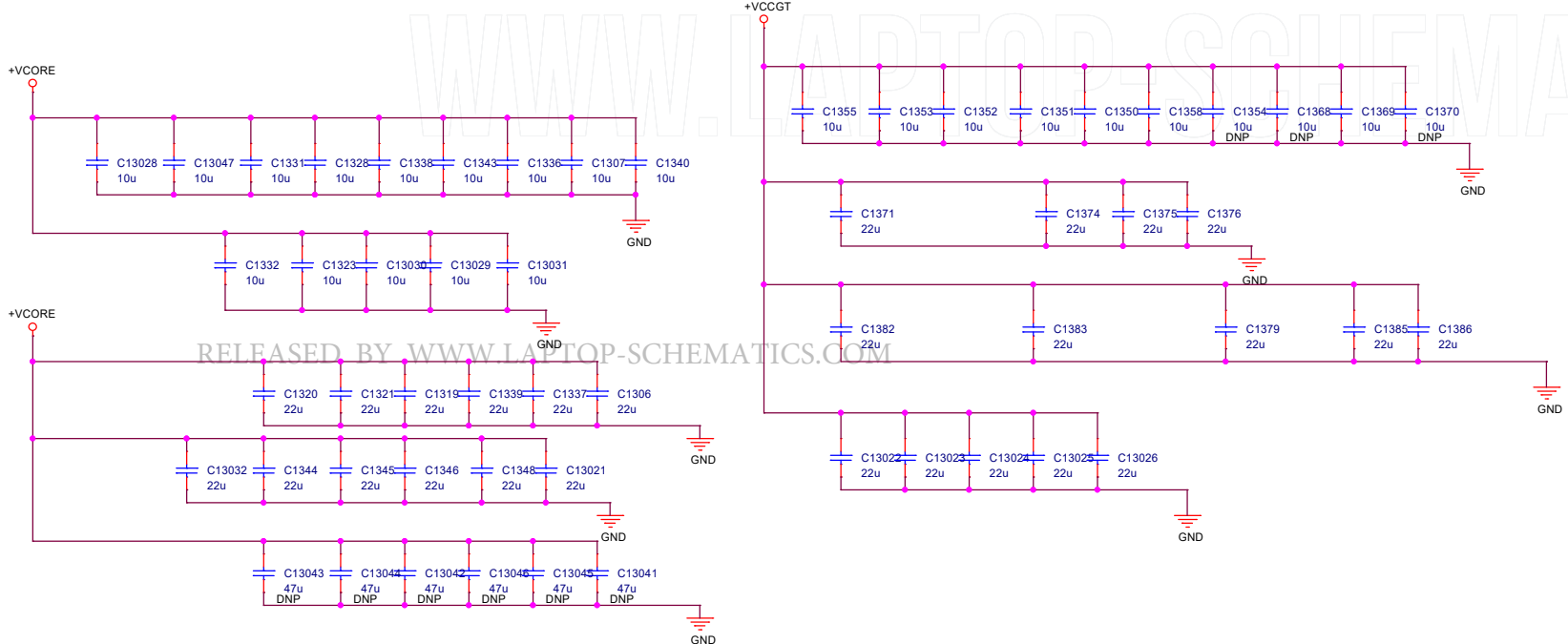
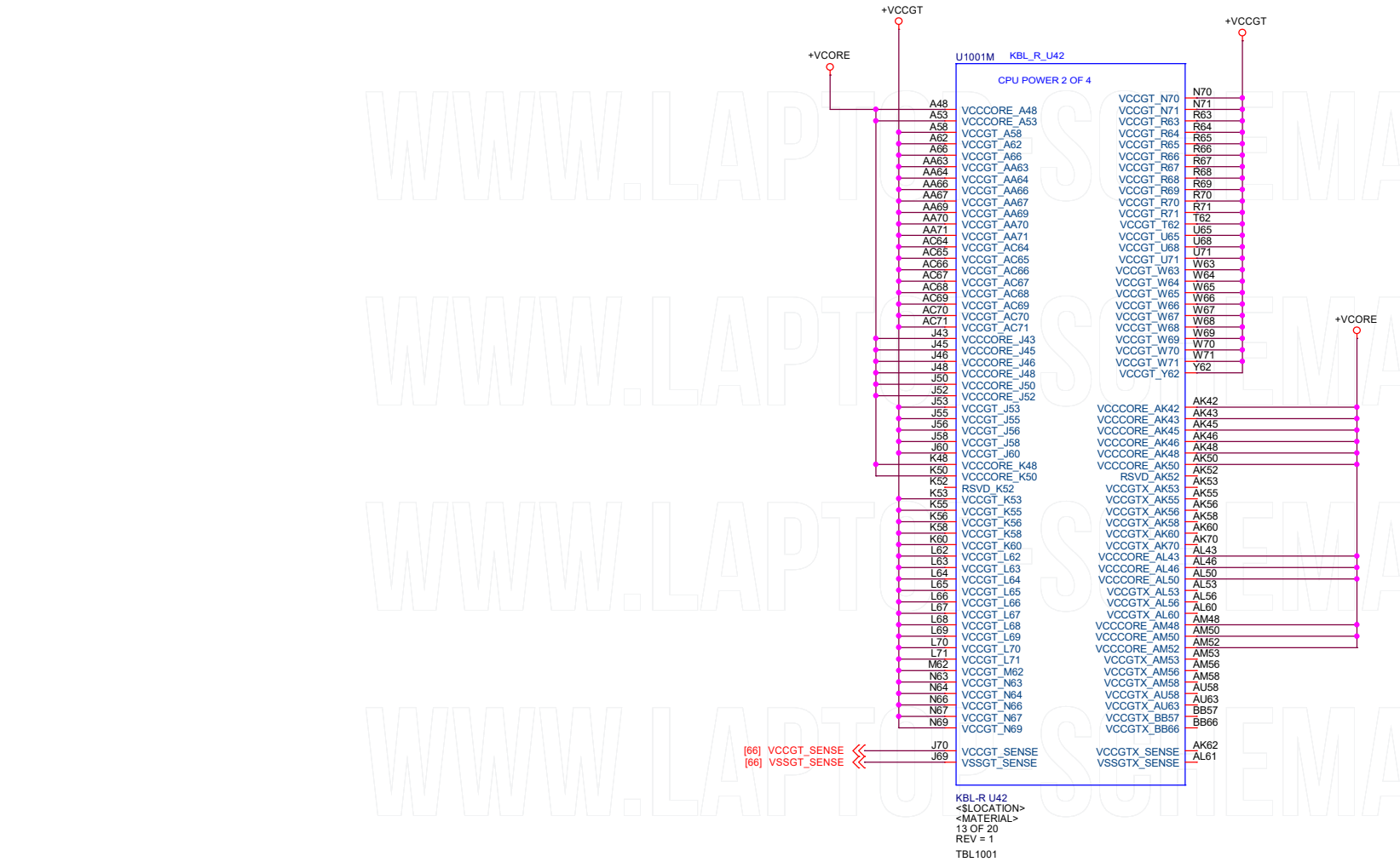


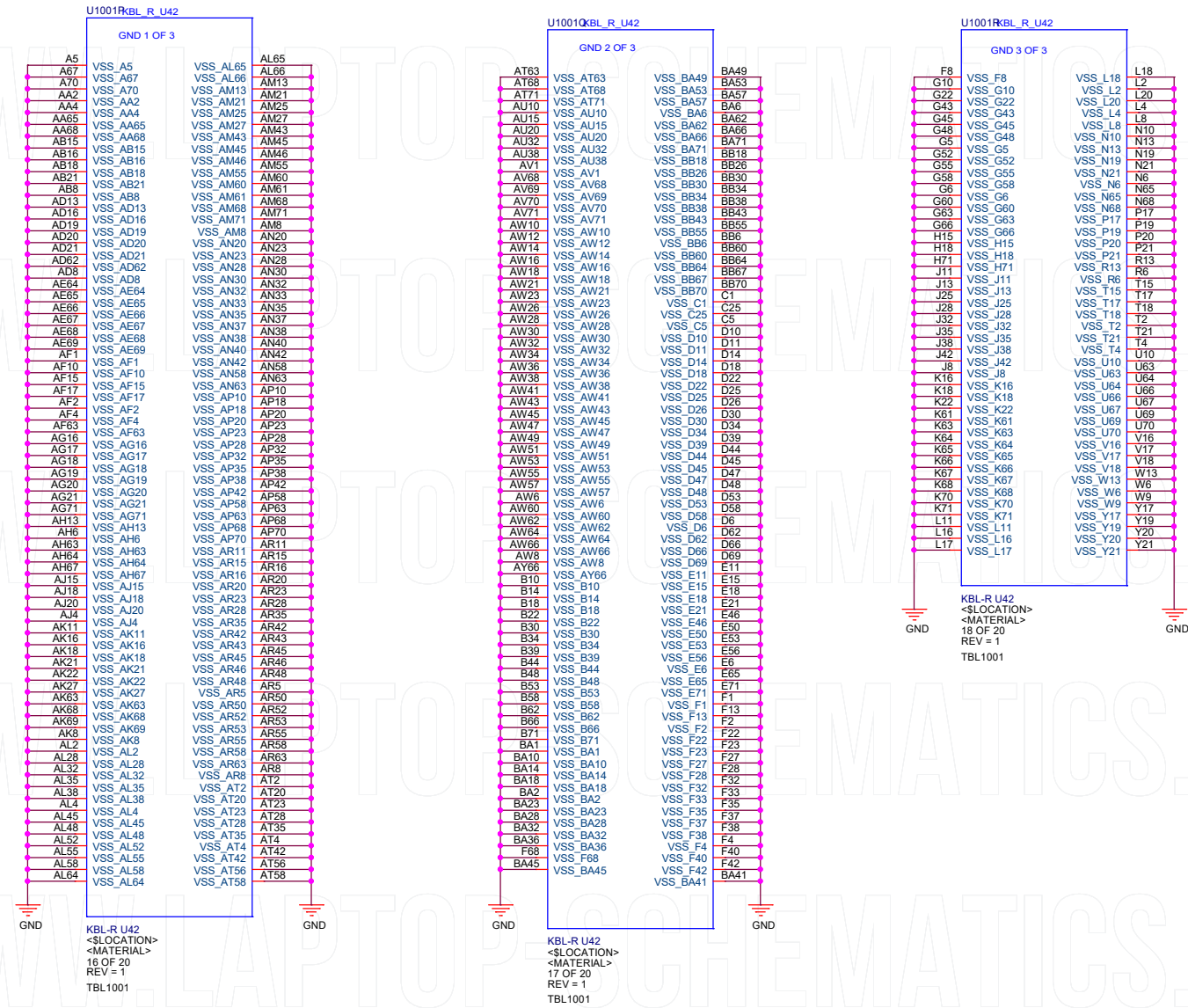


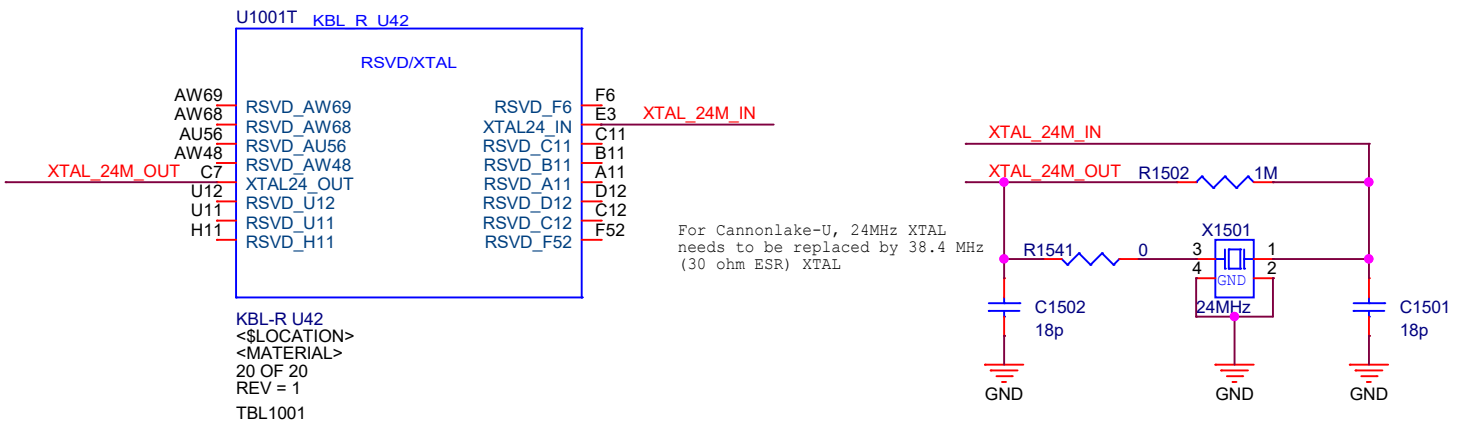
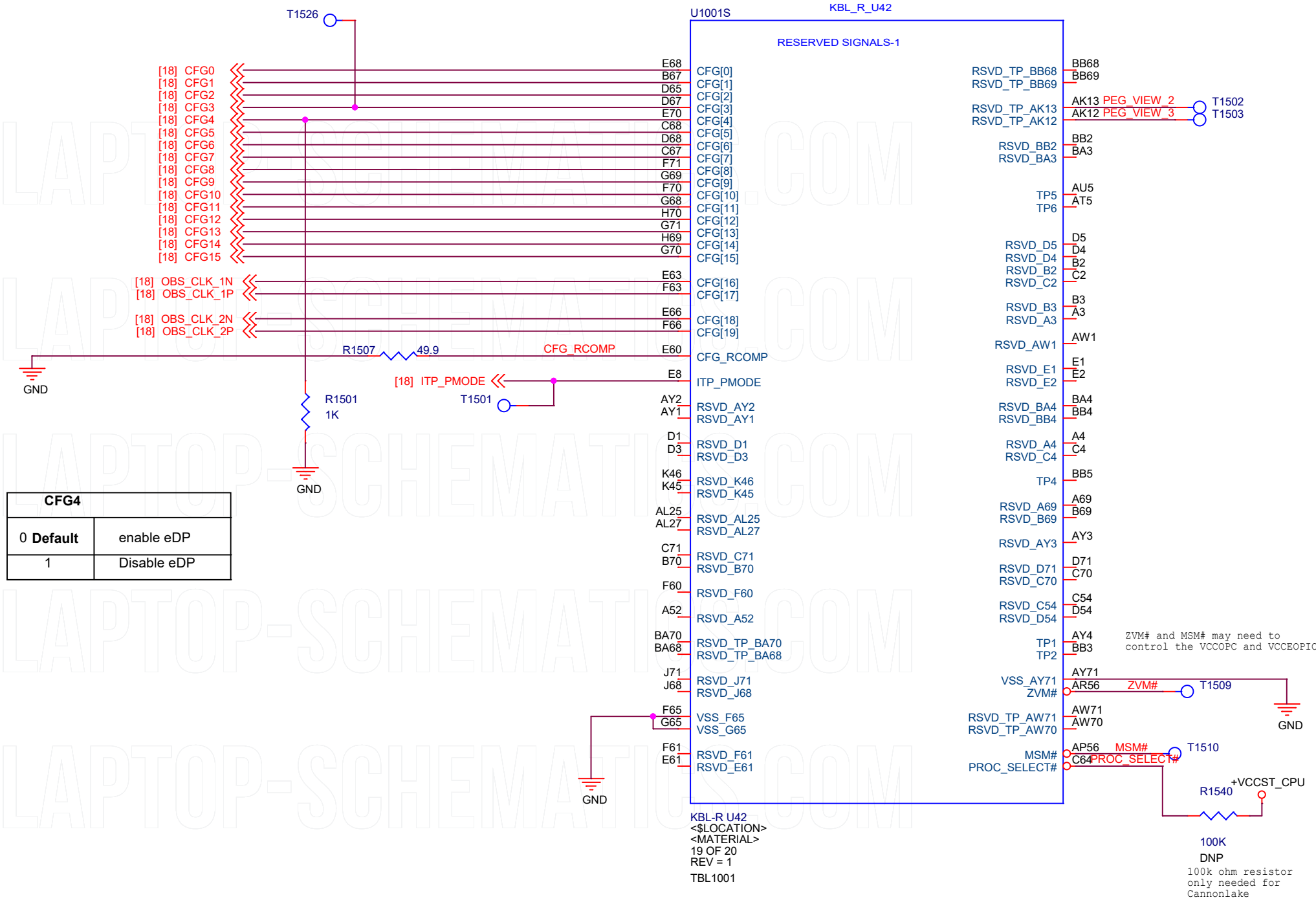


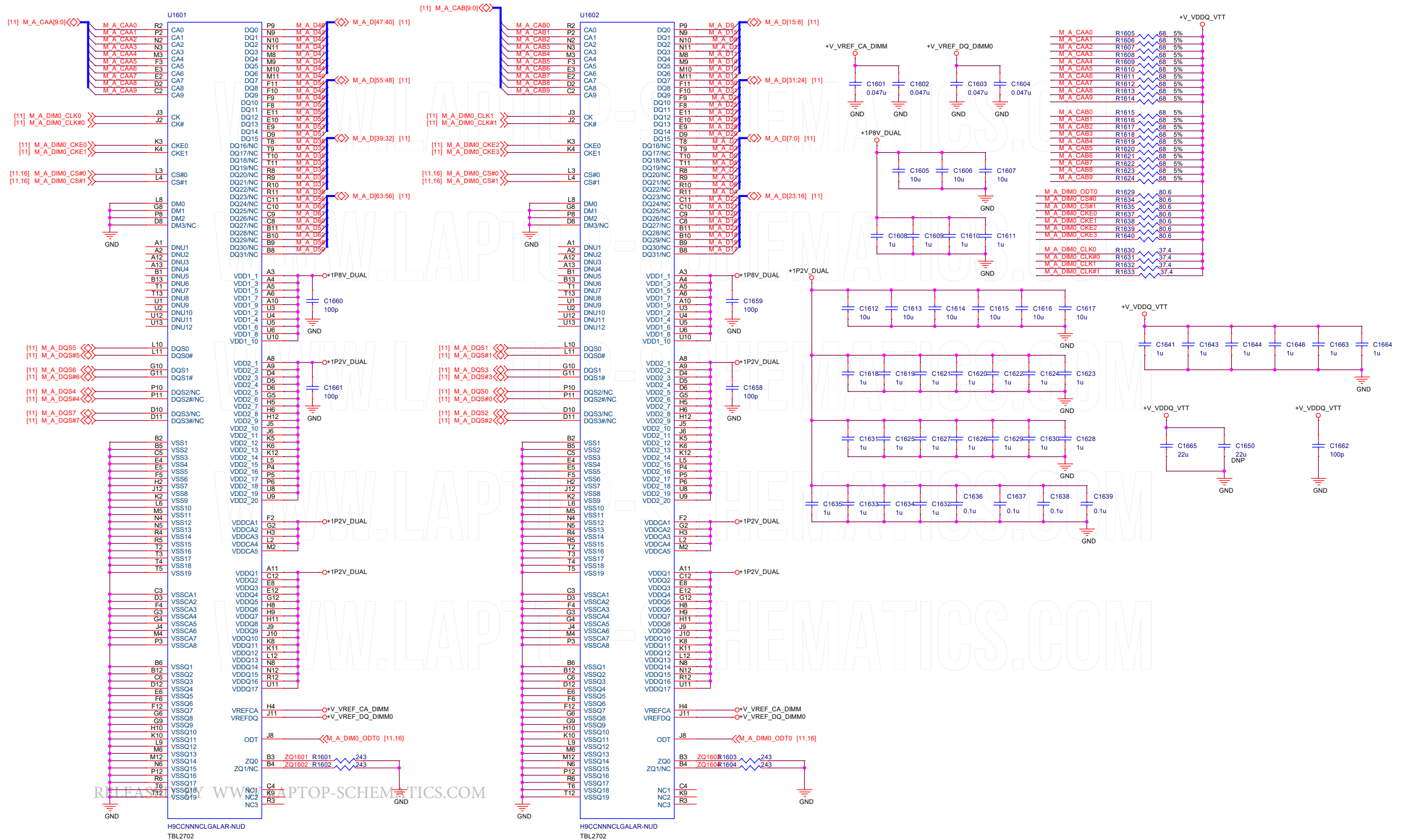
Do not route VccPLL, VccSTG, VccPLL OC closest adjacent layer over any power net other than ground.



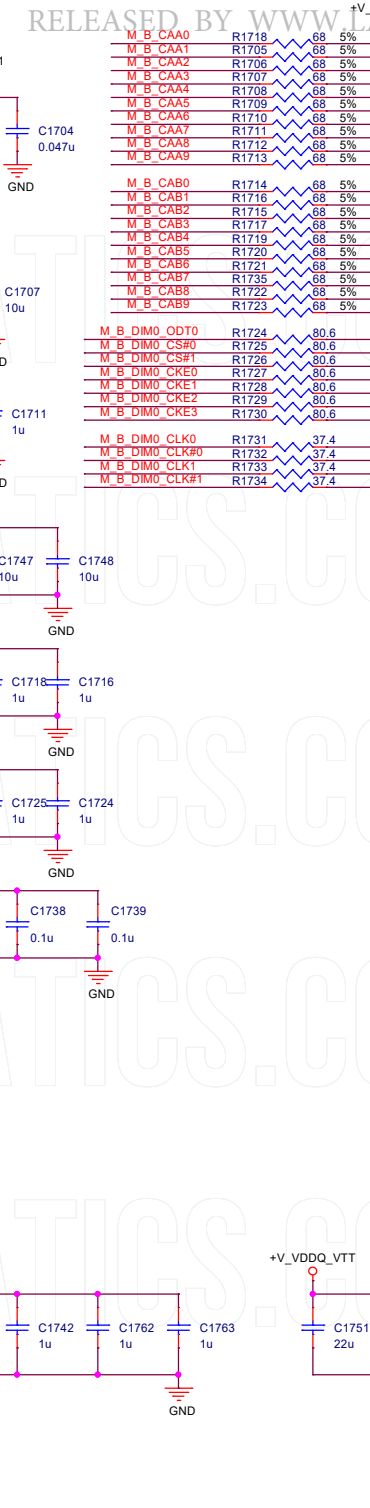
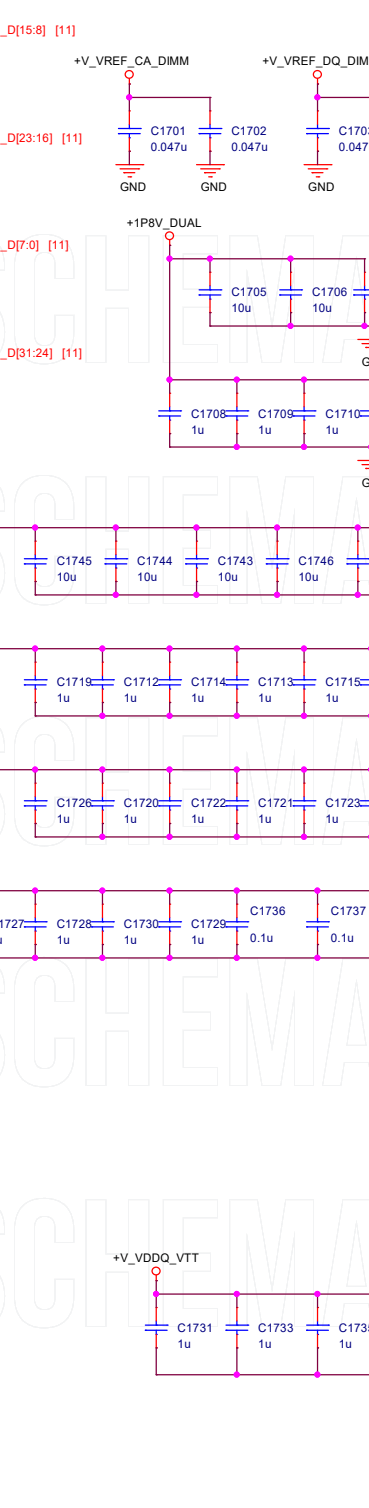
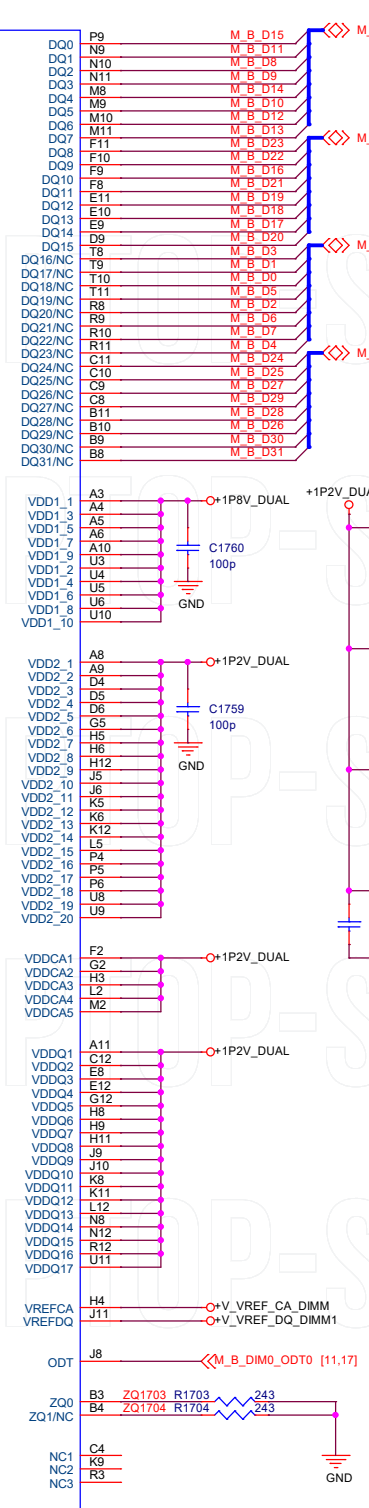
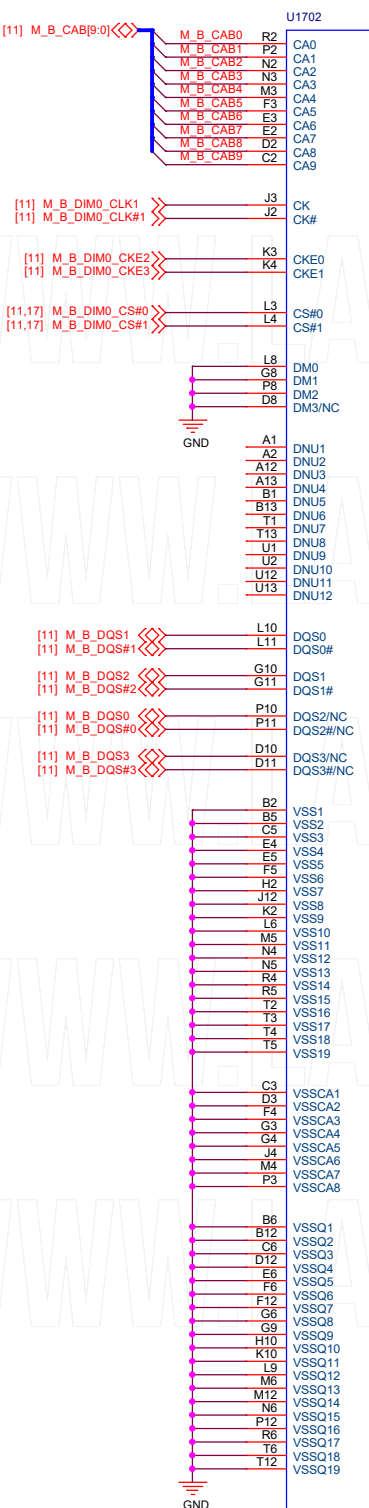
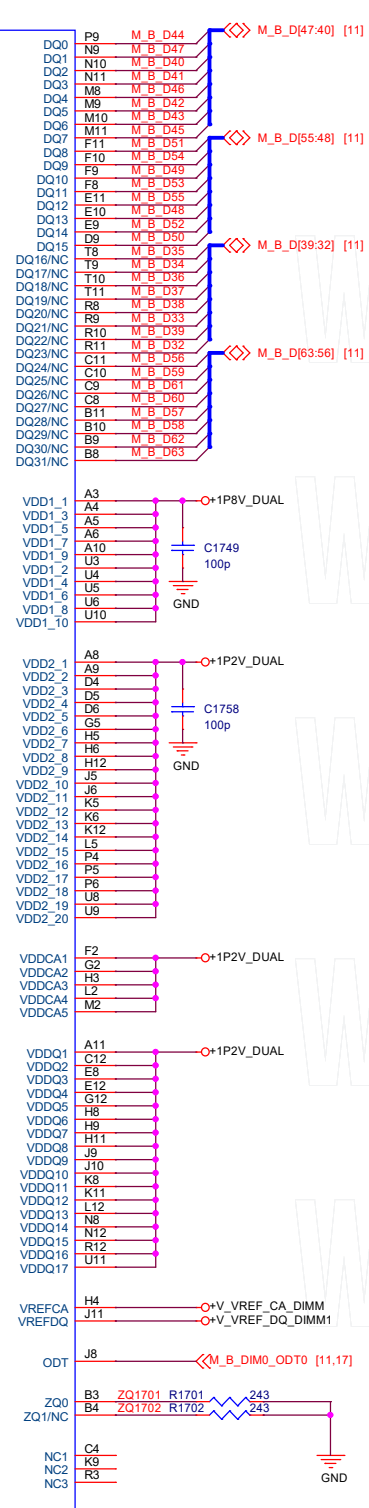
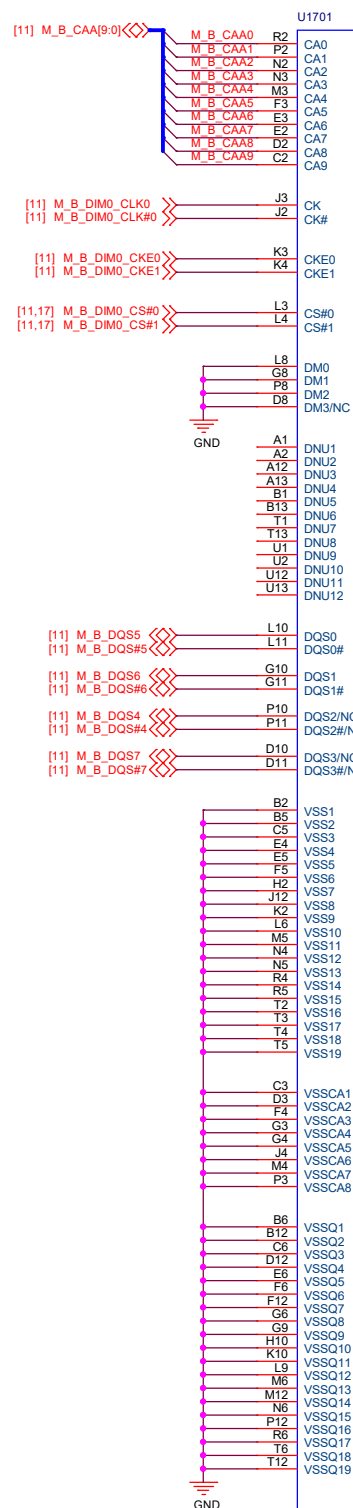










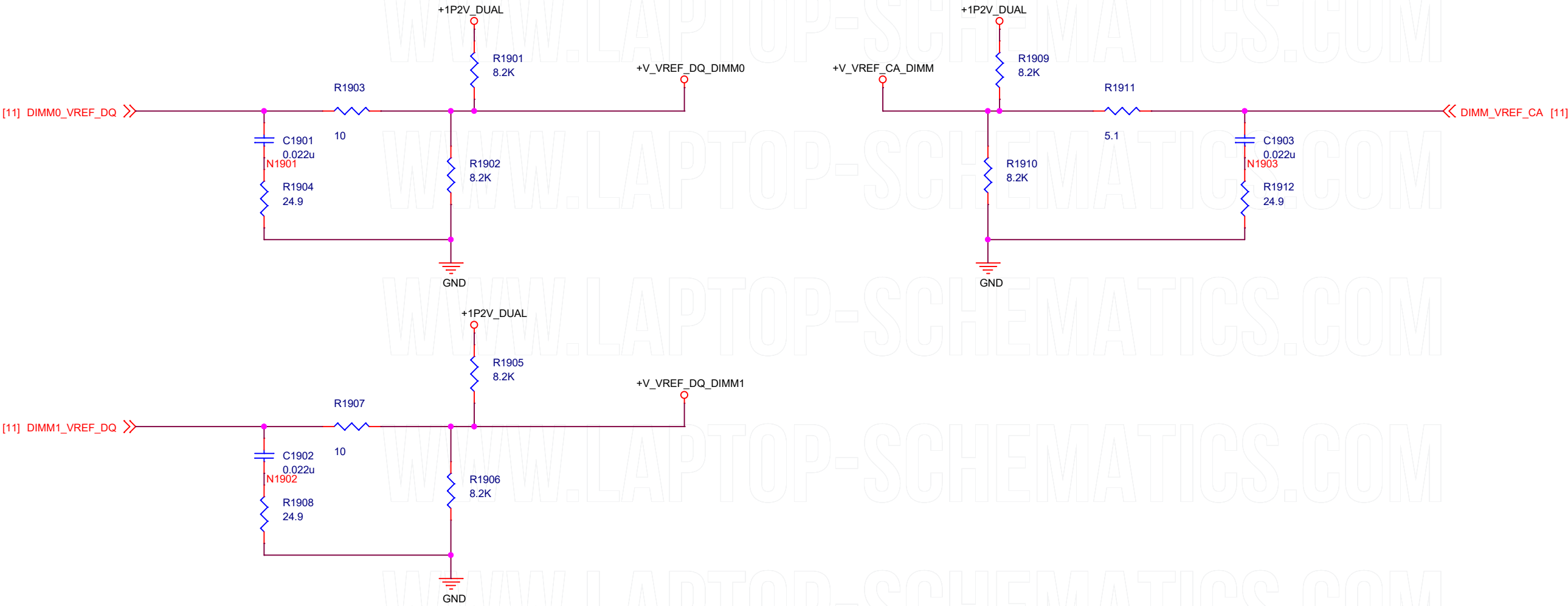




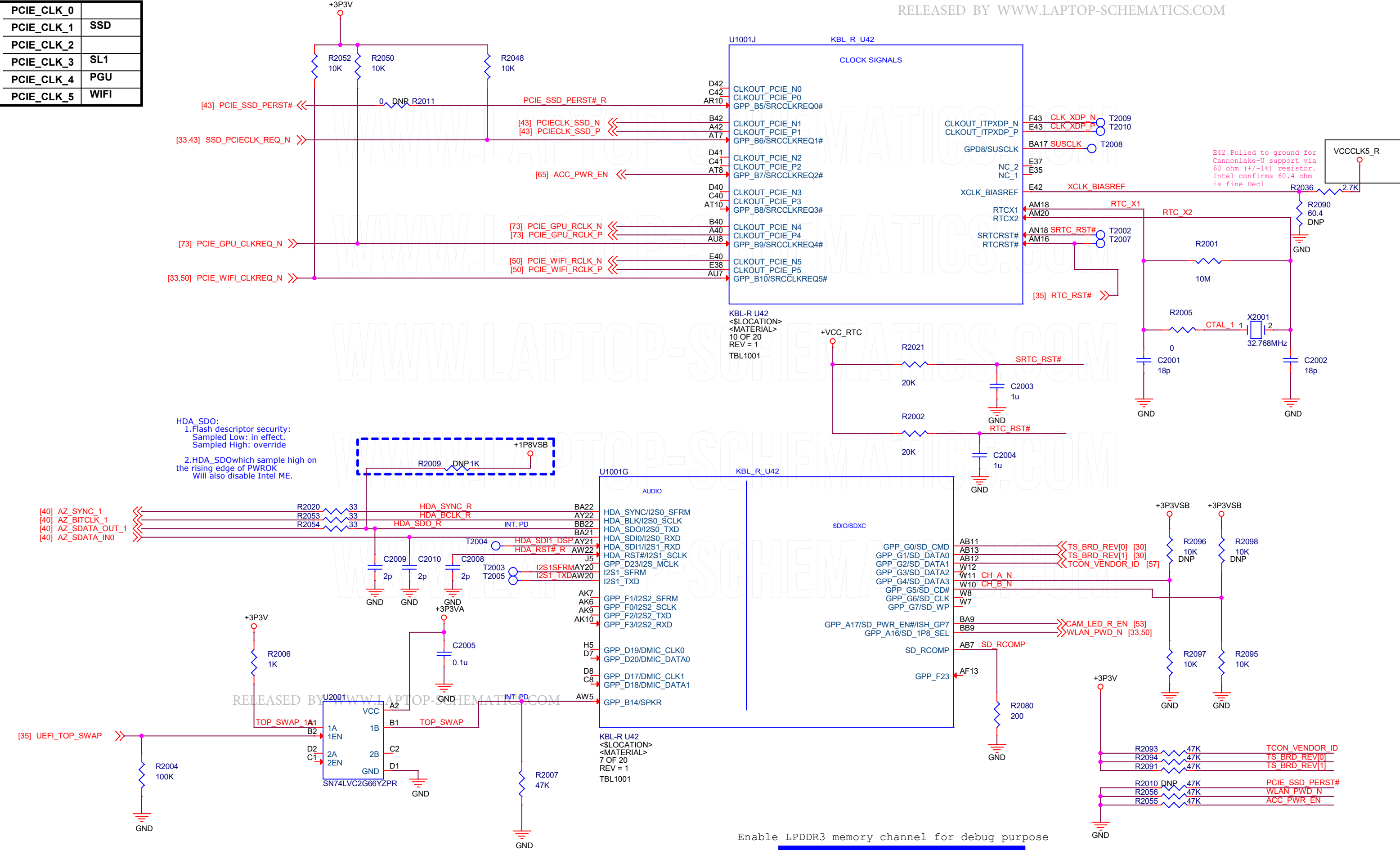


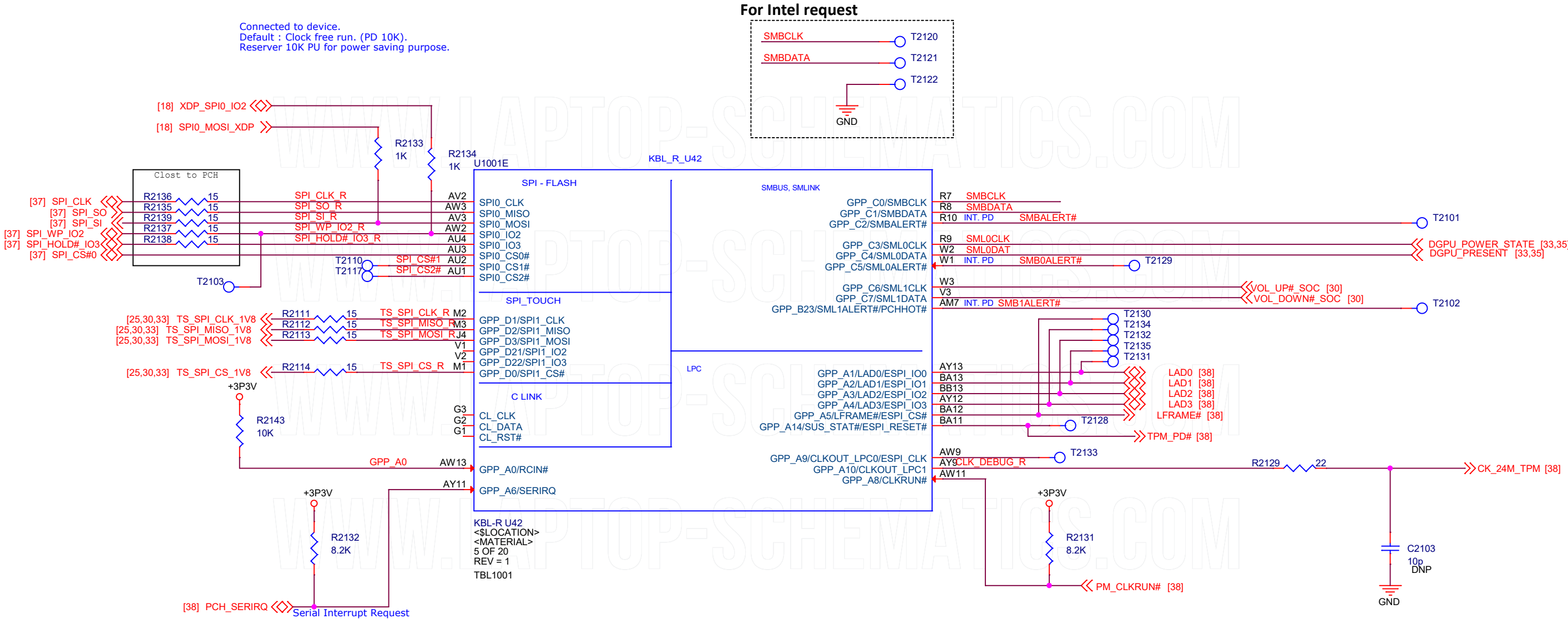
# LPDDR3 Vref

M3: CPU driven VREF path is stuffed be default.  
M1: VREF\_DQ driven by a Voltage Divider Network during Processor power-off



PCIE_CLK_0	
PCIE_CLK_1	SSD
PCIE_CLK_2	
PCIE_CLK_3	SL1
PCIE_CLK_4	PGU
PCIE_CLK_5	WIFI

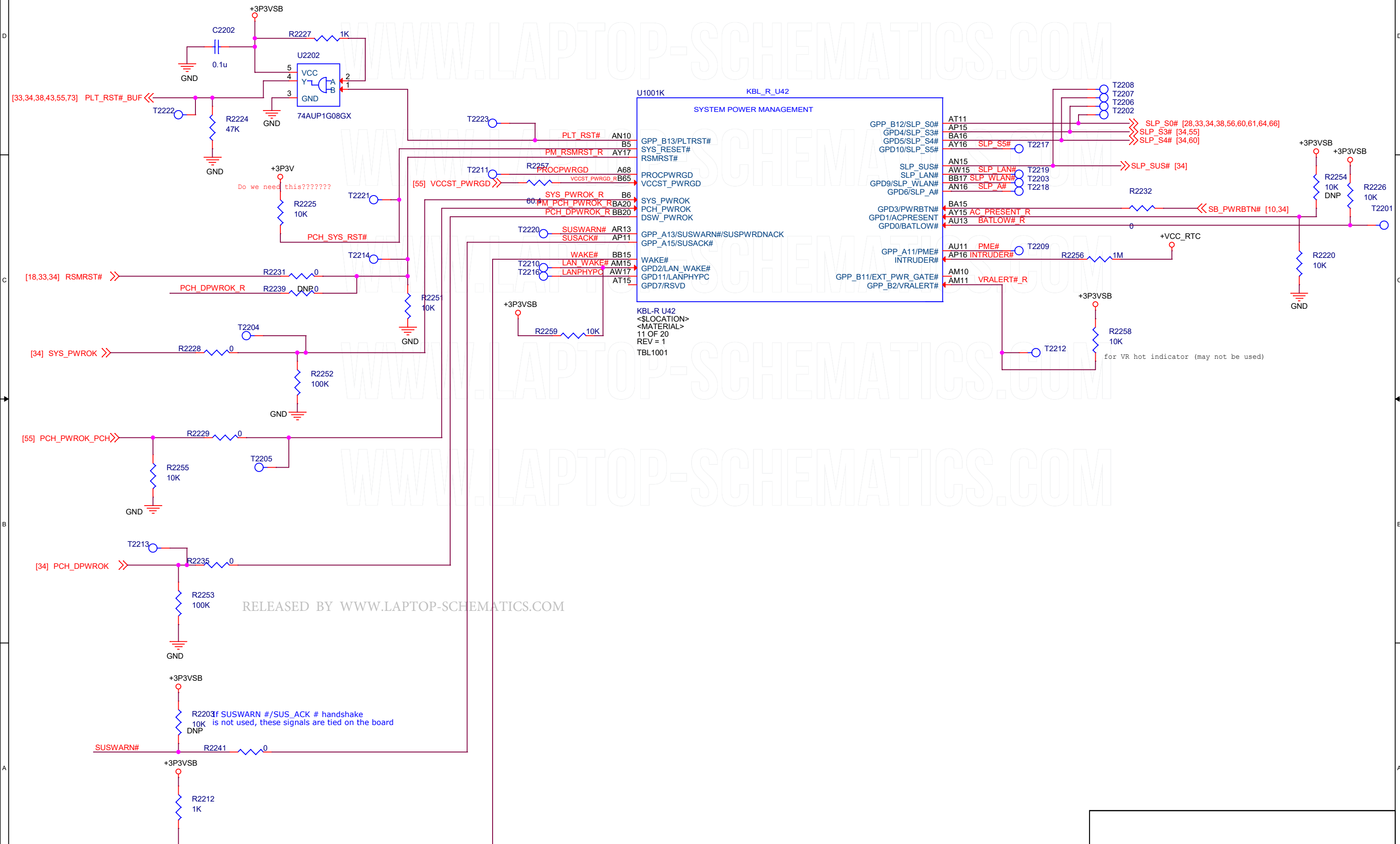




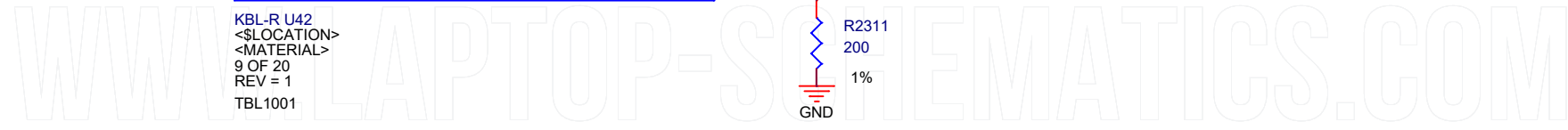
GPP_C2/SMBALERT#	
0 Default	Disable ME crypto TLS
1	Enable ME crypto TLS

GPP_C5/SML0ALERT#	
0 Default	LPC (EC)
1	eSPI (EC)





Will be removed after check CSI



KBL-R U42  
<LOCATION>  
<MATERIAL>  
9 OF 20  
REV = 1  
TBL1001

R2311  
200  
1%  
GND

U1001H KBL\_R\_U42

PCIE/USB3/SATA

SSIC / USB3

PCIE WIFI

[50] PCIE\_WIFI\_RXN1  
[50] PCIE\_WIFI\_RXP1  
[50] PCIE\_WIFI\_TXN1  
[50] PCIE\_WIFI\_TXP1

PCIE GPU

[71,73] PCIE\_GPU\_RN5\_L0  
[71,73] PCIE\_GPU\_RP5\_L0  
[73] PCIE\_GPU\_TN5\_L0  
[73] PCIE\_GPU\_TP5\_L0  
[71,73] PCIE\_GPU\_RN5\_L1  
[71,73] PCIE\_GPU\_RP5\_L1  
[73] PCIE\_GPU\_TN5\_L1  
[73] PCIE\_GPU\_TP5\_L1  
[71,73] PCIE\_GPU\_RN5\_L2  
[71,73] PCIE\_GPU\_RP5\_L2  
[73] PCIE\_GPU\_TN5\_L2  
[73] PCIE\_GPU\_TP5\_L2  
[71,73] PCIE\_GPU\_RN5\_L3  
[71,73] PCIE\_GPU\_RP5\_L3  
[73] PCIE\_GPU\_TN5\_L3  
[73] PCIE\_GPU\_TP5\_L3  
[43] PCIE\_SSD\_RN0  
[43] PCIE\_SSD\_RP0  
[43] PCIE\_SSD\_TN0  
[43] PCIE\_SSD\_TP0  
[43] PCIE\_SSD\_RN1  
[43] PCIE\_SSD\_RP1  
[43] PCIE\_SSD\_TN1  
[43] PCIE\_SSD\_TP1

SSD GPU

[43] PCIE\_SSD\_RN2  
[43] PCIE\_SSD\_RP2  
[43] PCIE\_SSD\_TN2  
[43] PCIE\_SSD\_TP2  
[43] PCIE\_SSD\_RN3  
[43] PCIE\_SSD\_RP3  
[43] PCIE\_SSD\_TN3  
[43] PCIE\_SSD\_TP3

H13 PCIE1\_RXN/USB3\_5\_RXN  
G13 PCIE1\_RXP/USB3\_5\_RXP  
B17 PCIE1\_TXN/USB3\_5\_TXN  
A17 PCIE1\_TXP/USB3\_5\_TXP  
G11 PCIE2\_RXN/USB3\_6\_RXN  
F11 PCIE2\_RXP/USB3\_6\_RXP  
D16 PCIE2\_TXN/USB3\_6\_TXN  
C16 PCIE2\_TXP/USB3\_6\_TXP  
H16 PCIE3\_RXN  
G16 PCIE3\_RXP  
D17 PCIE3\_TXN  
C17 PCIE3\_TXP  
G15 PCIE4\_RXN  
F15 PCIE4\_RXP  
B19 PCIE4\_TXN  
A19 PCIE4\_TXP  
F16 PCIE5\_RXN  
E16 PCIE5\_RXP  
C19 PCIE5\_TXN  
D19 PCIE5\_TXP  
G18 PCIE6\_RXN  
F18 PCIE6\_RXP  
D20 PCIE6\_TXN  
C20 PCIE6\_TXP  
F20 PCIE7\_RXN/SATA0\_RXN  
E20 PCIE7\_RXP/SATA0\_RXP  
B21 PCIE7\_TXN/SATA0\_TXN  
A21 PCIE7\_TXP/SATA0\_TXP  
G21 PCIE8\_RXN/SATA1A\_RXN  
F21 PCIE8\_RXP/SATA1A\_RXP  
D21 PCIE8\_TXN/SATA1A\_TXN  
C21 PCIE8\_TXP/SATA1A\_TXP  
E22 PCIE9\_RXN  
E23 PCIE9\_RXP  
B23 PCIE9\_TXN  
A23 PCIE9\_TXP  
F25 PCIE10\_RXN  
E25 PCIE10\_RXP  
D23 PCIE10\_TXN  
C23 PCIE10\_TXP  
F5 PCIE\_RCOMP\_N  
E5 PCIE\_RCOMP\_P  
D56 PROC\_PRDY#  
D61 PROC\_PREQ#  
BB11 GPP\_A7/PIRQA#  
E28 PCIE11\_RXN/SATA1B\_RXN  
E27 PCIE11\_RXP/SATA1B\_RXP  
D24 PCIE11\_TXN/SATA1B\_TXN  
C24 PCIE11\_TXP/SATA1B\_TXP  
E30 PCIE12\_RXN/SATA2\_RXN  
F30 PCIE12\_RXP/SATA2\_RXP  
A25 PCIE12\_TXN/SATA2\_TXN  
B25 PCIE12\_TXP/SATA2\_TXP

USB3\_1\_RXN  
USB3\_1\_RXP  
USB3\_1\_TXN  
USB3\_1\_TXP  
USB3\_2\_RXN/SSIC\_RXN  
USB3\_2\_RXP/SSIC\_RXP  
USB3\_2\_TXN/SSIC\_TXN  
USB3\_2\_TXP/SSIC\_TXP  
USB3\_3\_RXN  
USB3\_3\_RXP  
USB3\_3\_TXN  
USB3\_3\_TXP  
USB3\_4\_RXN  
USB3\_4\_RXP  
USB3\_4\_TXN  
USB3\_4\_TXP

H8 USB3\_CONN\_RXN1 [45]  
G8 USB3\_CONN\_RXP1 [45]  
C13 USB3\_CONN\_TXN1 [45]  
D13 USB3\_CONN\_TXP1 [45]

USB3.0 T to B

J10 USB3\_3\_RXN  
H10 USB3\_3\_RXP  
B15 USB3\_3\_TXN C2402 0.1u  
A15 USB3\_3\_TXP C2401 0.1u

USB3\_A\_RX\_DEBUG\_IN\_N [33]  
USB3\_A\_RX\_DEBUG\_IN\_P [33]  
USB3\_A\_TX\_DEBUG\_OUT\_N [33]  
USB3\_A\_TX\_DEBUG\_OUT\_P [33]

For Software DCI checking

E10 USB3\_SL1\_RXN4 [71]  
F10 USB3\_SL1\_RXP4 [71]  
C15 USB3\_SL1\_TXN4 [71]  
D15 USB3\_SL1\_TXP4 [71]

USB3.0 SL1

AB9 USB2\_CONN\_D- [45]  
AB10 USB2\_CONN\_D+ [45]

USB T to B

AD6 USB2N\_2  
AD7 USB2P\_2  
AH3 USB2N\_3  
AJ3 USB2P\_3  
AD9 USB2N\_4  
AD10 USB2P\_4

SL1

AJ1 USB2N\_5  
AJ2 USB2P\_5  
AF6 USB2N\_6  
AF7 USB2P\_6

BT

AH1 USB2N\_7  
AH2 USB2P\_7  
AF8 USB2N\_8  
AF9 USB2P\_8

ACC radio

AG1 USB2N\_9  
AG2 USB2P\_9  
AH7 USB2N\_10  
AH8 USB2P\_10

AB6 USB2\_COMP  
AG3 USB2\_ID  
AG4 USB2\_VBUSSENSE

A9 GPP\_E9/USB2\_OC0#  
C9 GPP\_E10/USB2\_OC1#  
D9 GPP\_E11/USB2\_OC2#  
B9 GPP\_E12/USB2\_OC3#

J1 GPP\_E4/DEVSLP0  
J2 GPP\_E5/DEVSLP1  
J3 GPP\_E6/DEVSLP2

H2 GPP\_E0/SATAXPCIE0/SATAGP0  
H3 GPP\_E1/SATAXPCIE1/SATAGP1  
G4 GPP\_E2/SATAXPCIE2/SATAGP2

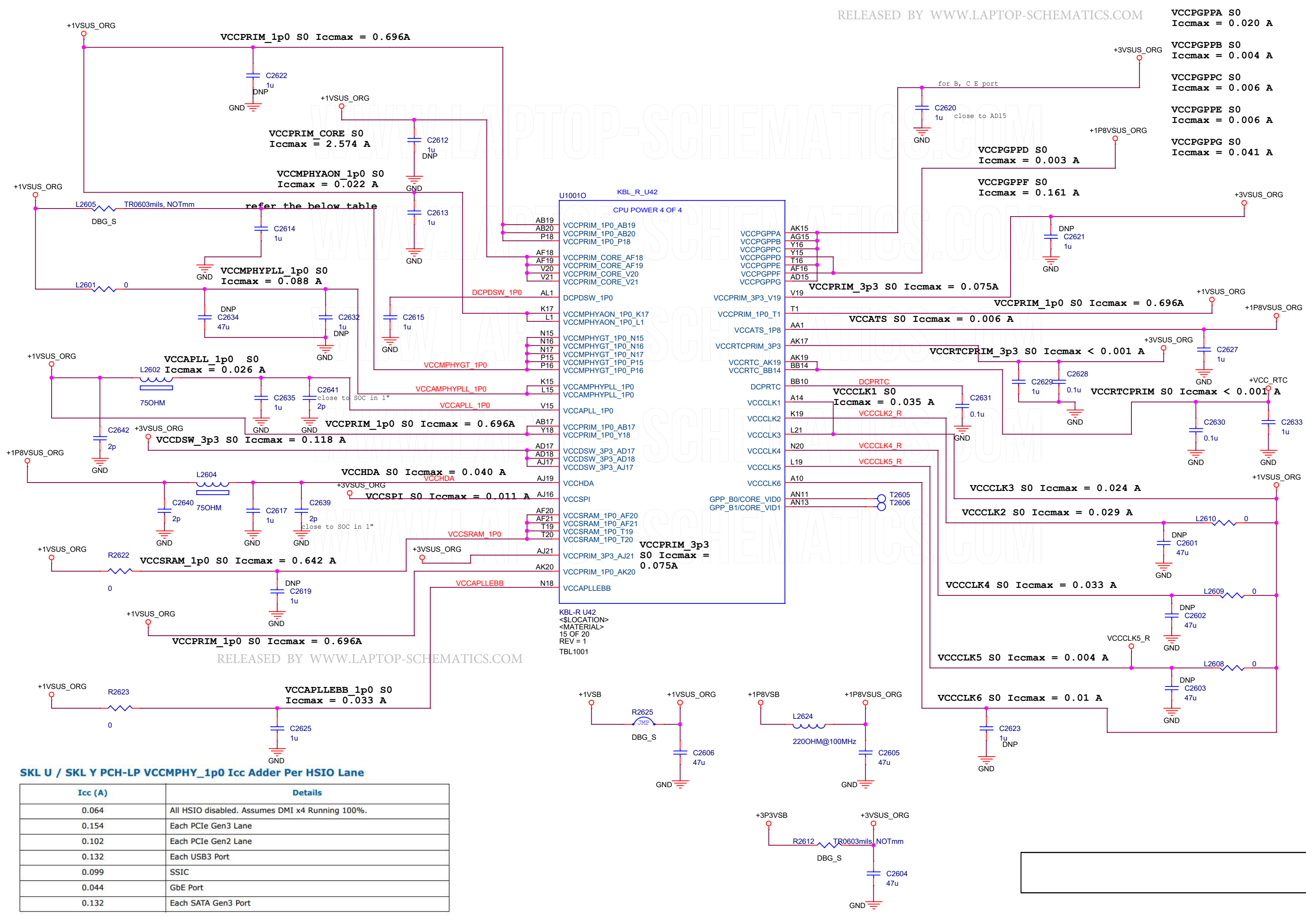
H1 GPP\_E8/SATALED#

KBL-R U42  
<LOCATION>  
<MATERIAL>  
8 OF 20  
REV = 1  
TBL1001









VCCPGPPA S0  
Iccmax = 0.020 A

VCCPGPPB S0  
Iccmax = 0.004 A

VCCPGPPC S0  
Iccmax = 0.006 A

VCCPGPPE S0  
Iccmax = 0.006 A

VCCPGPPG S0  
Iccmax = 0.041 A

VCCPGPPD S0  
Iccmax = 0.003 A

VCCPGPPF S0  
Iccmax = 0.161 A

VCCPRIM\_3p3 S0 Iccmax = 0.075A

VCCPRIM\_1p0 S0 Iccmax = 0.696A

VCCATS S0 Iccmax = 0.006 A

VCCRTCPRIM\_3p3 S0 Iccmax < 0.001 A

VCCCLK1 S0  
Iccmax = 0.035 A

VCCRTCPRIM S0 Iccmax < 0.001 A

VCCCLK3 S0 Iccmax = 0.024 A

VCCCLK2 S0 Iccmax = 0.029 A

VCCCLK4 S0 Iccmax = 0.033 A

VCCCLK5 S0 Iccmax = 0.004 A

VCCCLK6 S0 Iccmax = 0.01 A

VCCPRIM\_3p3 S0 Iccmax = 0.075A

VCCPRIM\_CORE S0  
Iccmax = 2.574 A

VCCMPHYAON\_1p0 S0  
Iccmax = 0.022 A

VCCMPHYPLL\_1p0 S0  
Iccmax = 0.088 A

VCCAPLL\_1p0 S0  
Iccmax = 0.026 A

VCCPRIM\_1p0 S0 Iccmax = 0.696A

VCCDSW\_3p3 S0 Iccmax = 0.118 A

VCCCHDA S0 Iccmax = 0.040 A

VCCSPT S0 Iccmax = 0.011 A

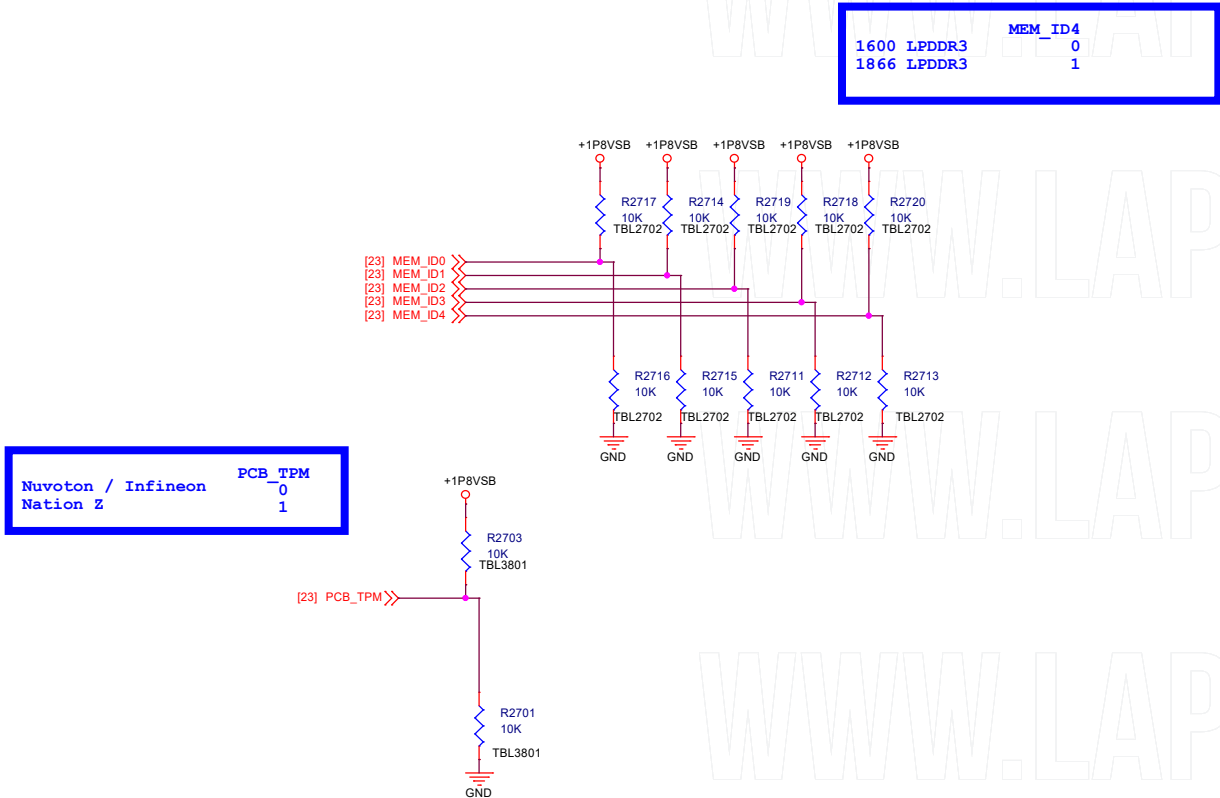
VCCSRAM\_1p0 S0 Iccmax = 0.642 A

VCCPRIM\_1p0 S0 Iccmax = 0.696A

VCCAPLLEBB\_1p0 S0  
Iccmax = 0.033 A

SKL U / SKL Y PCH-LP VCCMPHY\_1p0 Icc Adder Per HSIO Lane

Icc (A)	Details
0.064	All HSIO disabled. Assumes DMI x4 Running 100%.
0.154	Each PCIe Gen3 Lane
0.102	Each PCIe Gen2 Lane
0.132	Each USB3 Port
0.099	SSIC
0.044	GbE Port
0.132	Each SATA Gen3 Port



	MEM_ID1	MEM_ID0
Hynix 2znm	0	0
Samsung 20nm	0	1

	MEM_ID2	MEM_ID3
4GB	0	0
8GB	1	0
16GB	0	1

	PCBID4	PCB_ID3	PCB_ID2	PCB_ID1	PCB_ID0
EV3A	1	0	0	1	1
EV3B	1	0	1	1	0
DV	1	0	1	1	1
PV	1	1	0	0	0

	PCB_ID4
Gauntlet	0
Shield	1

TBL2701

Build	X861217-001 Qty (10K 0201)	PCH_Value	PCH_10K	PCH_NOSTUFF
EV3A	5	10011	R2721, R2710, R2709, R2706, R2704	R2722, R2707, R2705, R2708, R2702
	5	10100	R2721, R2710, R2705, R2708, R2702	R2722, R2707, R2709, R2706, R2704
	5	10101	R2721, R2710, R2705, R2708, R2704	R2722, R2707, R2709, R2706, R2702
EV3B	5	10110	R2721, R2710, R2705,R2706, R2702	R2722, R2707, R2709, R2708, R2704
DV	5	10111	R2721, R2710, R2705,R2706, R2704	R2722, R2707, R2709, R2708, R2702
PV	5	11000	R2721, R2707, R2709, R2708, R2702	R2722, R2710, R2705, R2706, R2704

TBL2702

<b>H4GB 1866 2znm</b>	Hynix 8Gb 1866	H9CCNNN8GTALAR-NUD
Mem	M1008409-001	U1601,U1602,U1701,U1702
Res	X811791-001	R2720, R2716, R2715, R2711, R2712
NI	NO-STUFF	R2713, R2717, R2714, R2719, R2718
<b>H8GB 1866 2znm</b>	Hynix 16Gb 1866	H9CCNNNBJTALAR-NUD
Mem	M1008406-001	U1601,U1602,U1701,U1702
Res	X811791-001	R2720, R2716, R2715, R2719, R2712
NI	NO-STUFF	R2713, R2717, R2714, R2711, R2718
<b>S4GB 1866 D20</b>	Samsung 8Gb 1866	K4E8E324EB-EGCF000
Mem	X946149-001	U1601,U1602,U1701,U1702
Res	X811791-001	R2720, R2717, R2715, R2711, R2712
NI	NO-STUFF	R2713, R2716, R2714, R2719, R2718
<b>S8GB 1866 D20</b>	Samsung 16Gb 1866	K4E6E304EB-EGCF000
Mem	X946454-001	U1601,U1602,U1701,U1702
Res	X811791-001	R2720, R2717, R2715, R2719, R2712
NI	NO-STUFF	R2713, R2716, R2714, R2711, R2718
<b>S16GB 1866 D20</b>	Samsung 32Gb 1866	K4EBE304EB-EGCF000
Mem	X930118-001	U1601,U1602,U1701,U1702
Res	X811791-001	R2720, R2717, R2715, R2711, R2718
NI	NO-STUFF	R2713, R2716, R2714, R2719, R2712
<b>H16GB 1866 2znm</b>	Hynix 32Gb 1866	H9CCNNNCLGALAR-NUD
Mem	M1008421-001	U1601,U1602,U1701,U1702
Res	X811791-001	R2720, R2716, R2715, R2711, R2718
NI	NO-STUFF	R2713, R2717, R2714, R2719, R2712

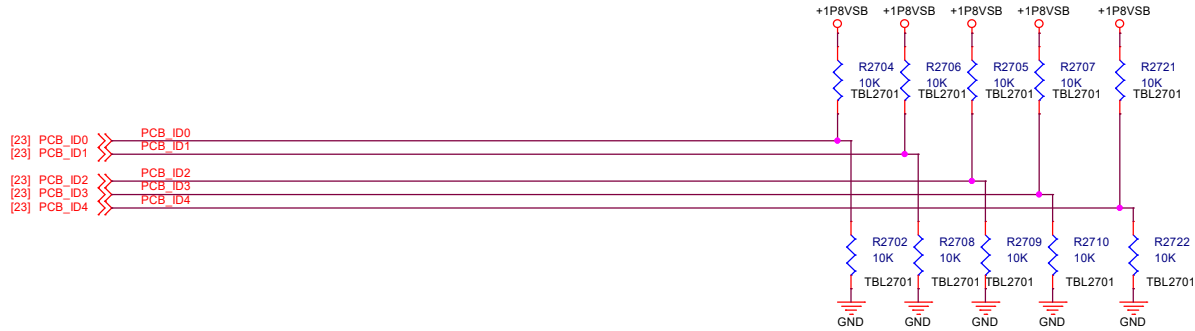
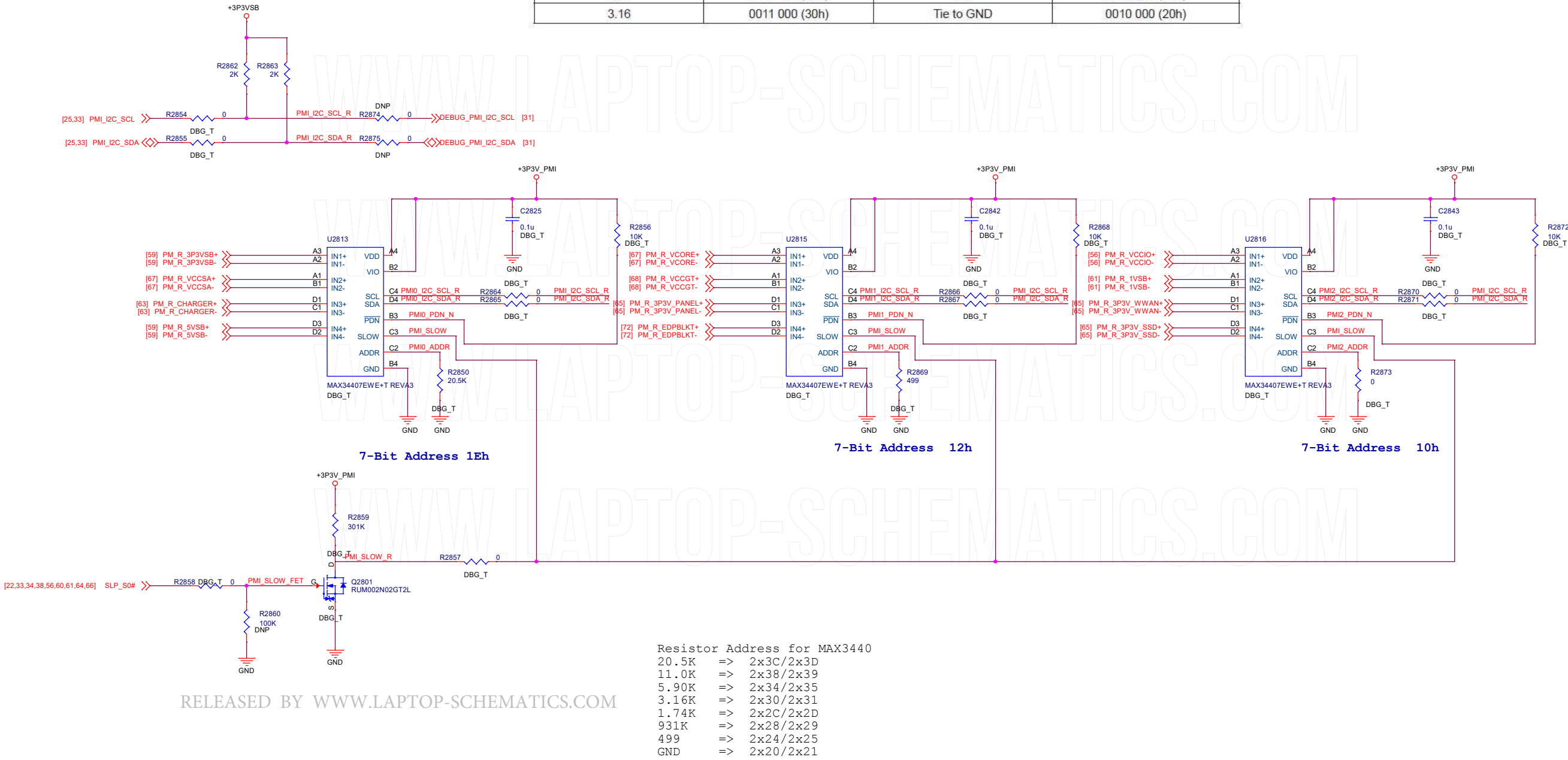
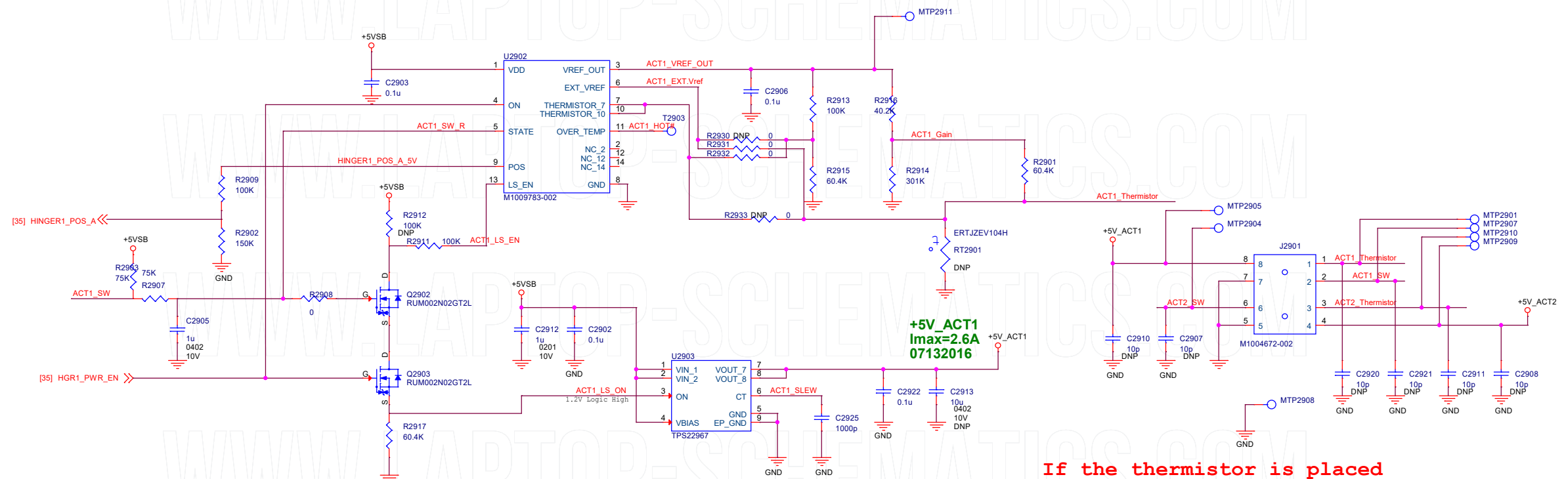


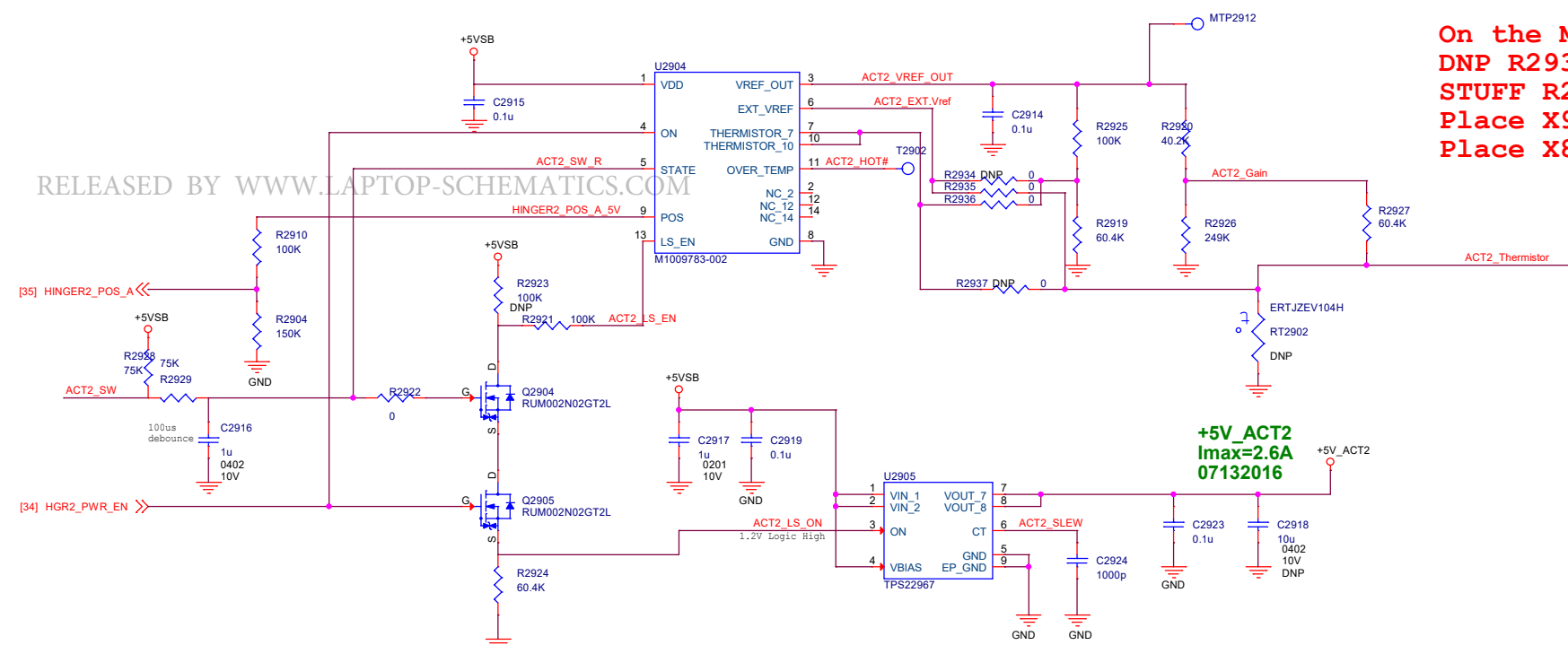
Table 5. SMBus Slave Address Select

RADDR (±1%) (kΩ)	SLAVE ADDRESS	RADDR (±1%) (Ω)	SLAVE ADDRESS
20.5	0011 110 (3Ch)	1.74k	0010 110 (2Ch)
11.0	0011 100 (38h)	931	0010 100 (28h)
5.90	0011 010 (34h)	442	0010 010 (24h)
3.16	0011 000 (30h)	Tie to GND	0010 000 (20h)





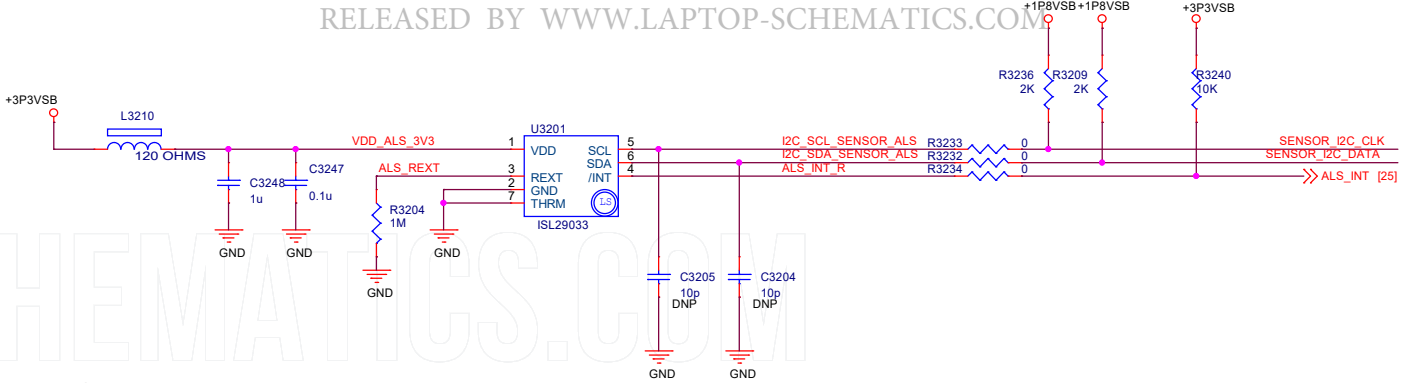
On the MB:  
DNP R2931, R2932, R2935, R2936  
STUFF R2930, R2933, R2934, R2937  
Place X930189-001 in R2901, R2927 locations  
Place X801411-001 in RT2901, RT2902 locations





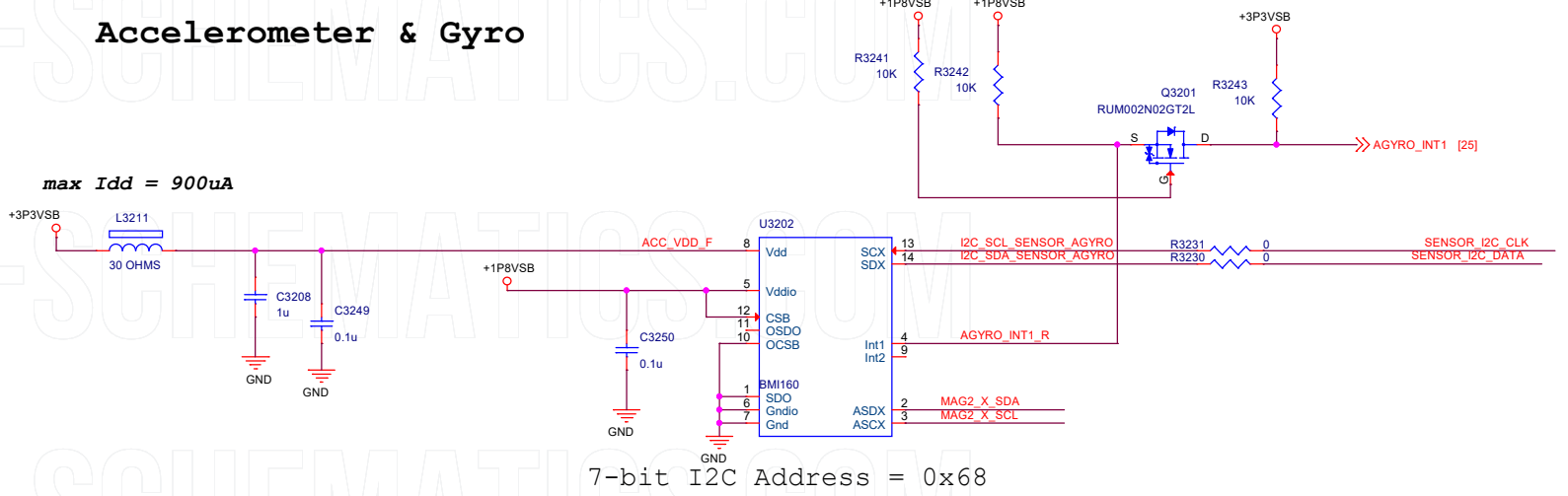






7-bit I2C Address = 0x44

### Accelerometer & Gyro



7-bit I2C Address = 0x68

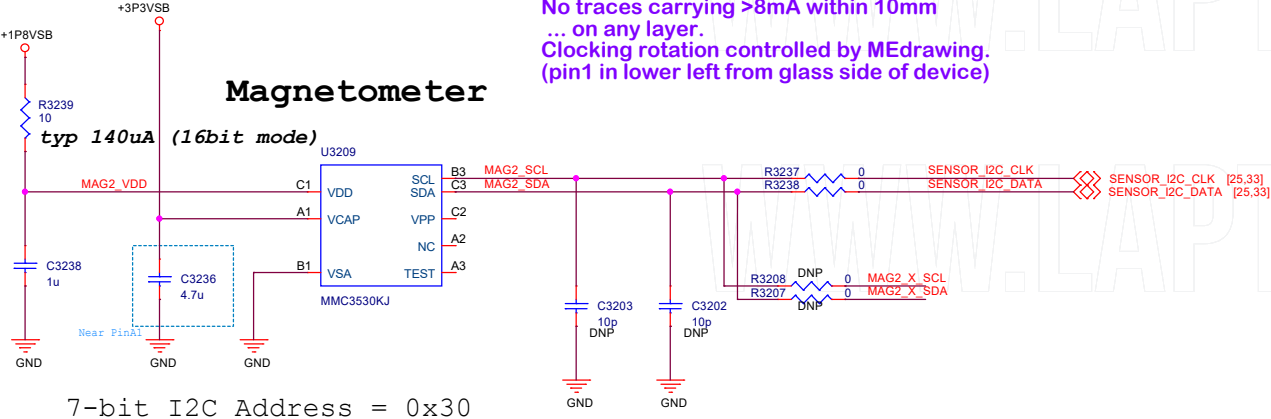
**Critical Layout Note for Mems devices:**

- No traces under part,
- No vias in pads or directly under part,
- All traces entering pads to be same width,
- All traces to enter pads at zero angle.

**Clocking rotation controlled by MEdrawing.**  
(+X Device & +X Surface vectors must be parallel w/same direction  
(i.e. if the part is located on the glass side of the PCB, the pin1 indicator dot should be in upper right corner)

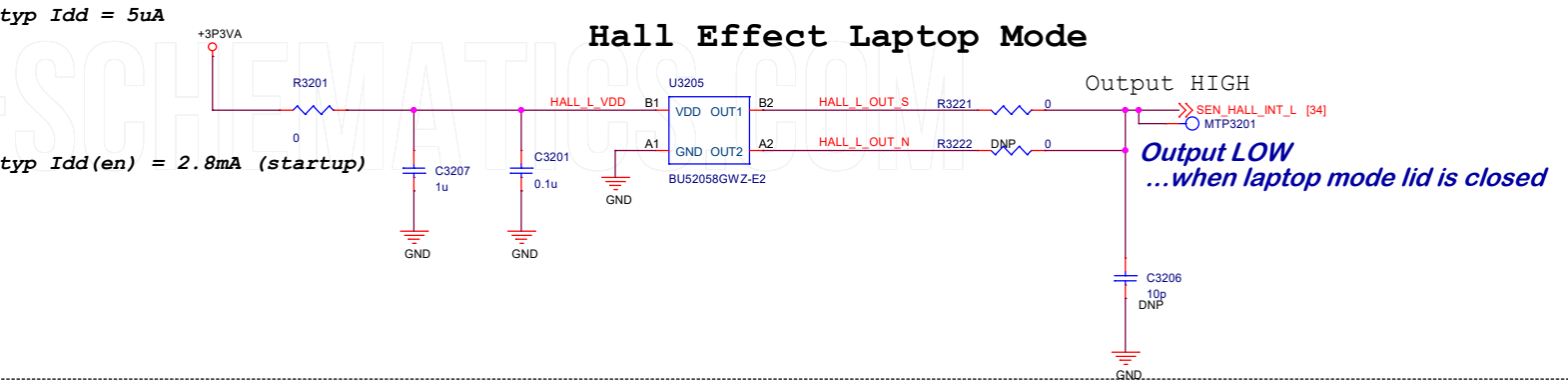
**Critical Layout Note:**  
Extremely sensitive to ferrous materials:  
Local ferrite bead to be >8mm remote  
No traces carrying >8mA within 10mm  
... on any layer.  
Clocking rotation controlled by MEdrawing.  
(pin1 in lower left from glass side of device)

### Magnetometer



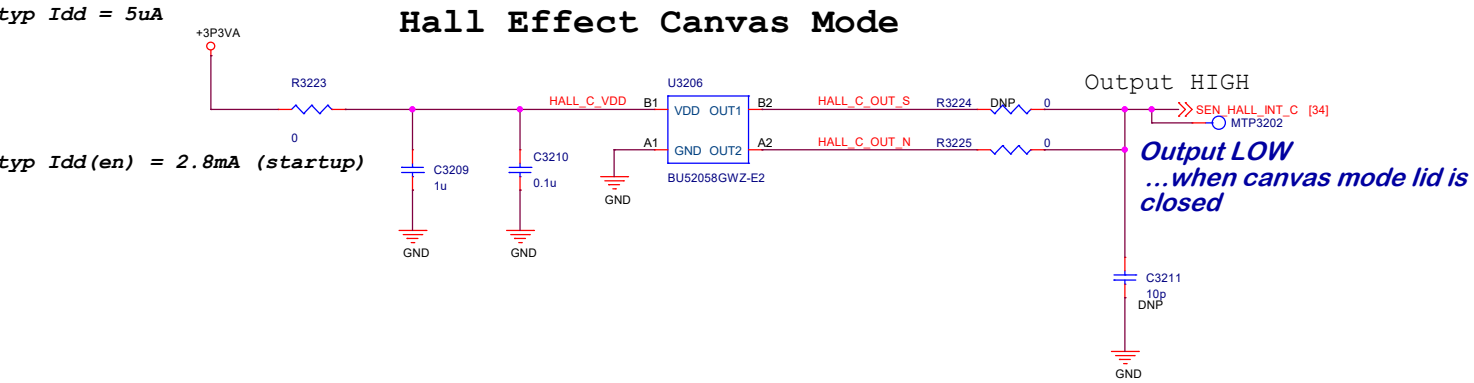
7-bit I2C Address = 0x30

### Hall Effect Laptop Mode



Output HIGH  
...when laptop mode lid is closed

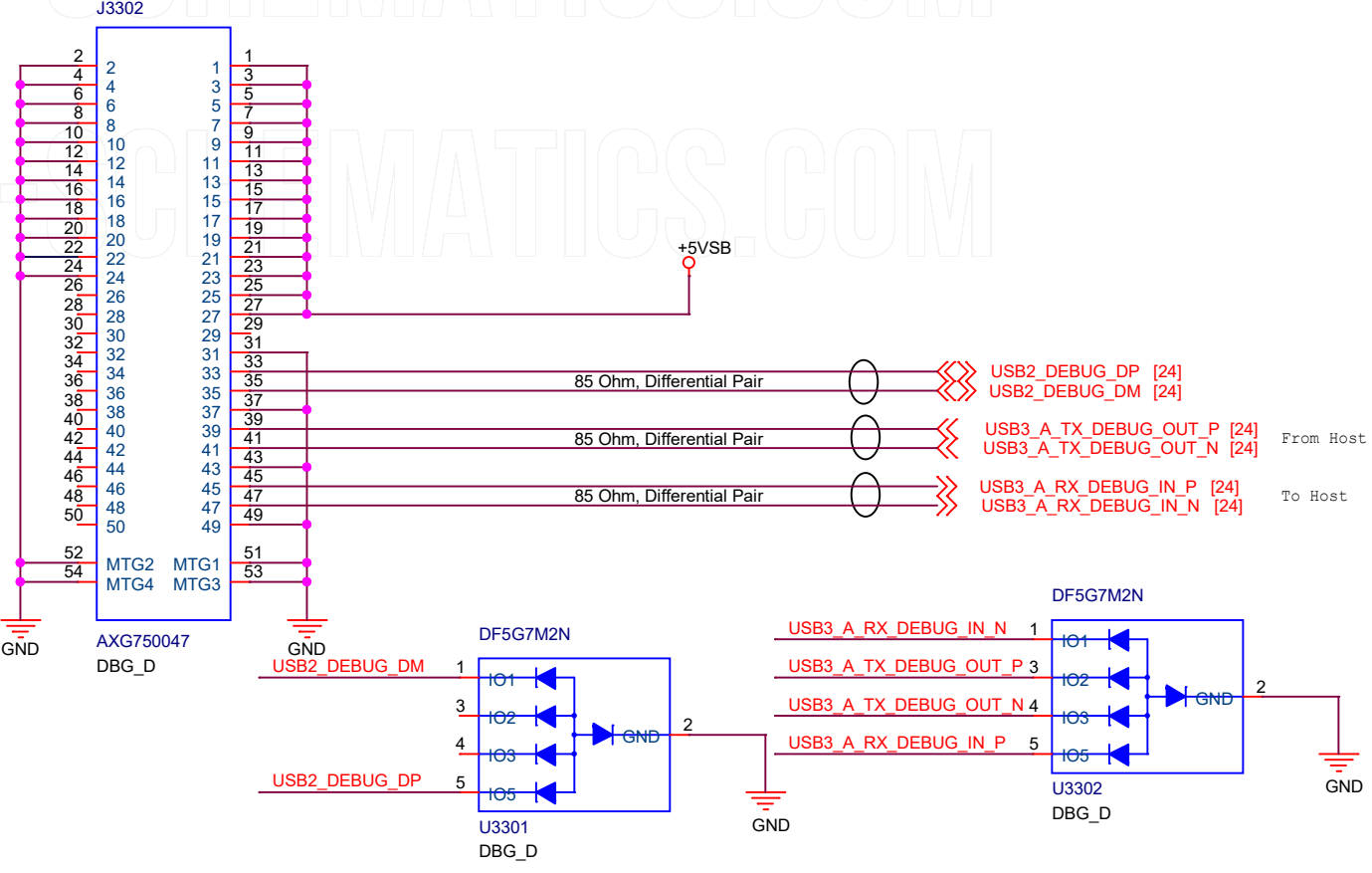
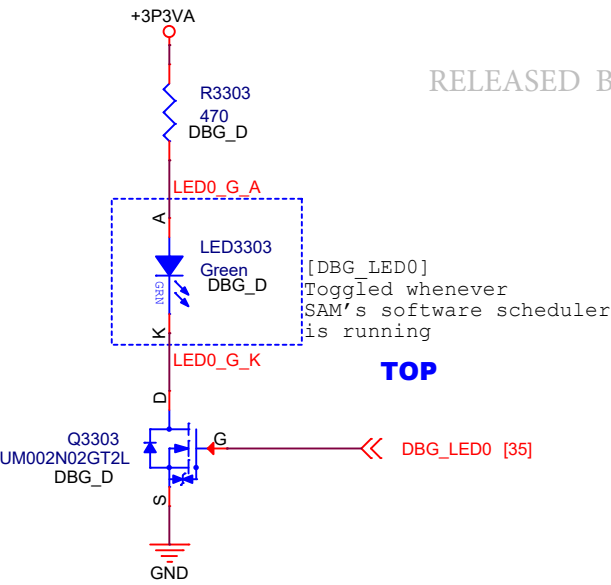
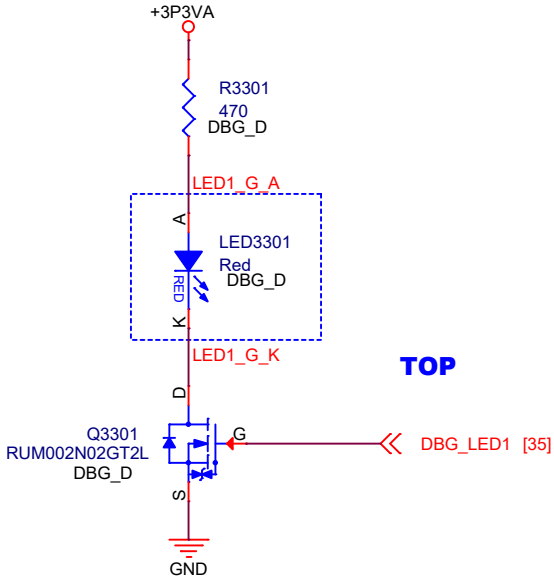
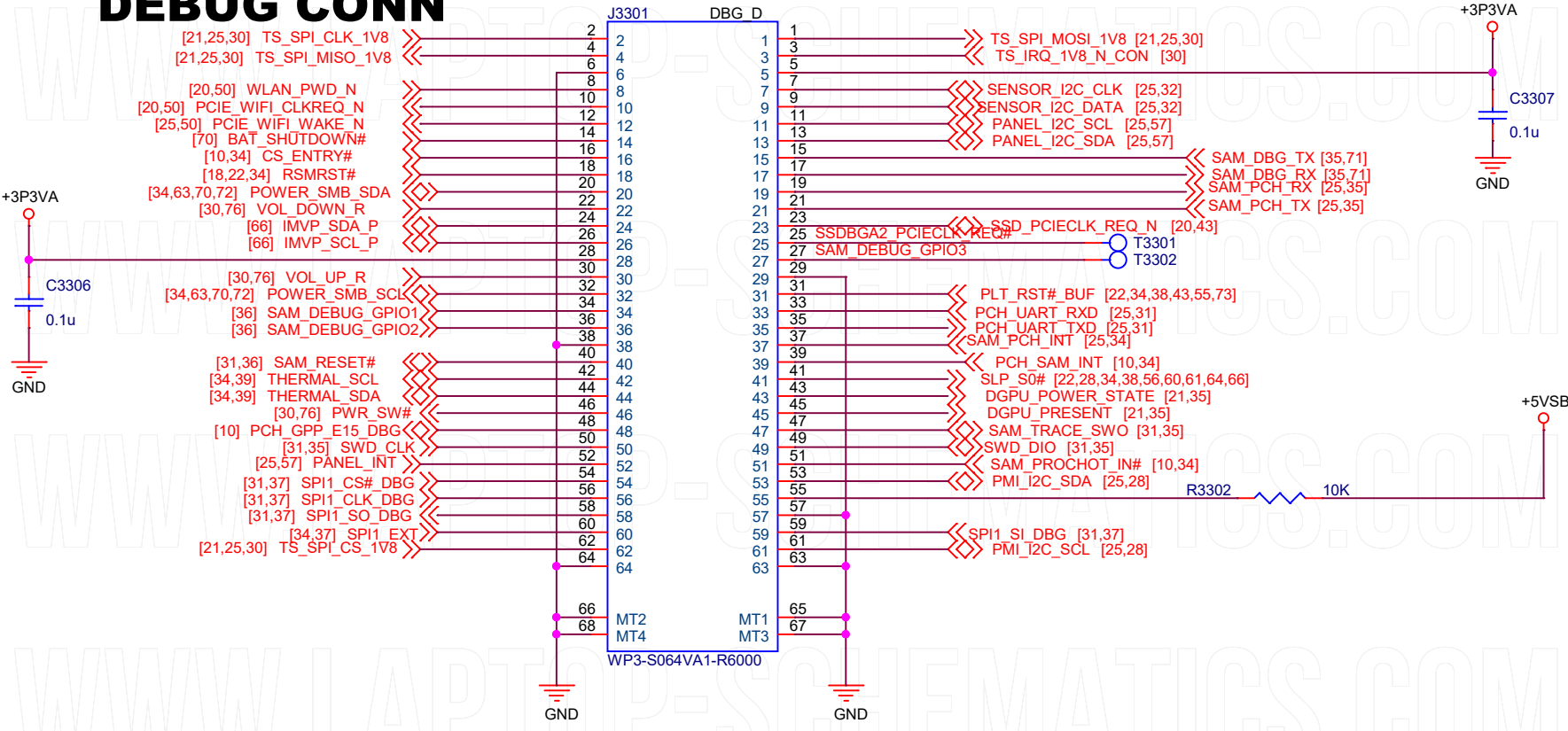
### Hall Effect Canvas Mode



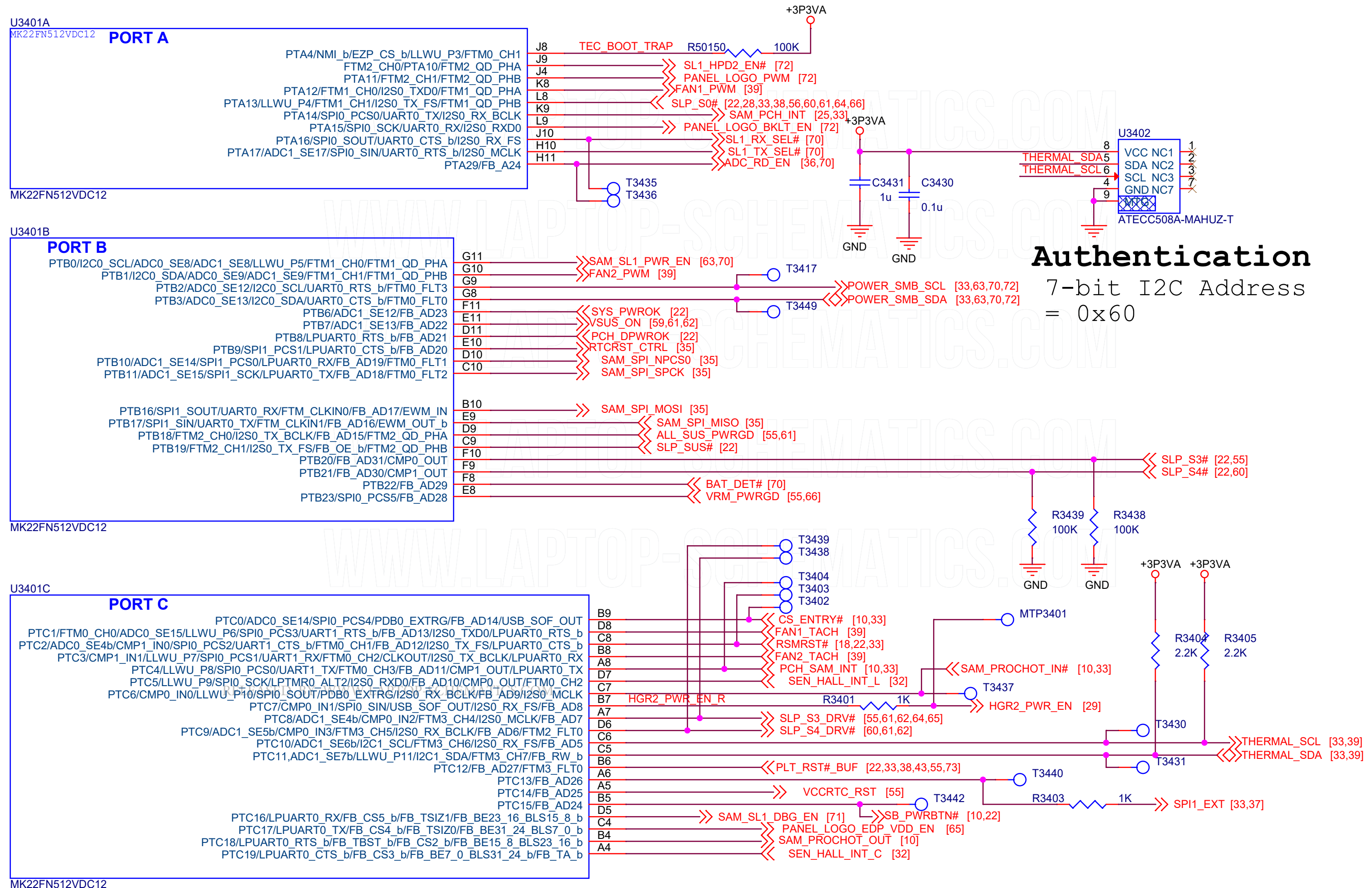
Output HIGH  
...when canvas mode lid is closed

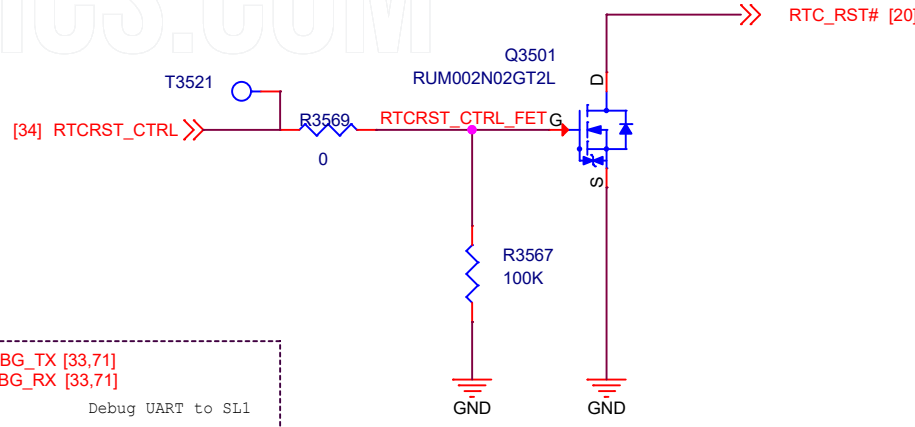
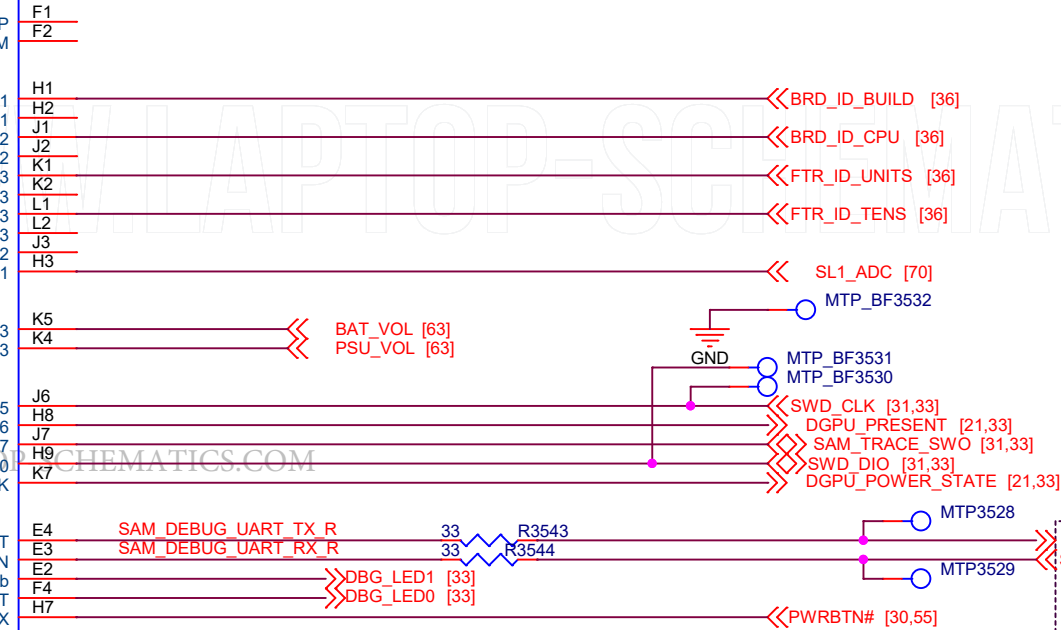
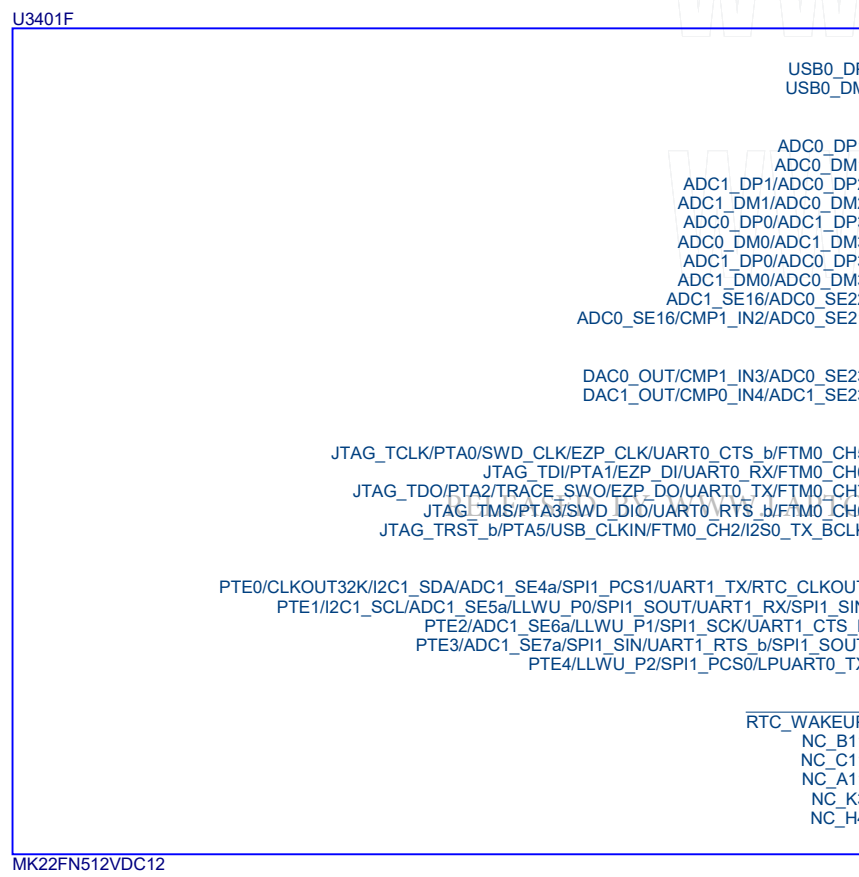
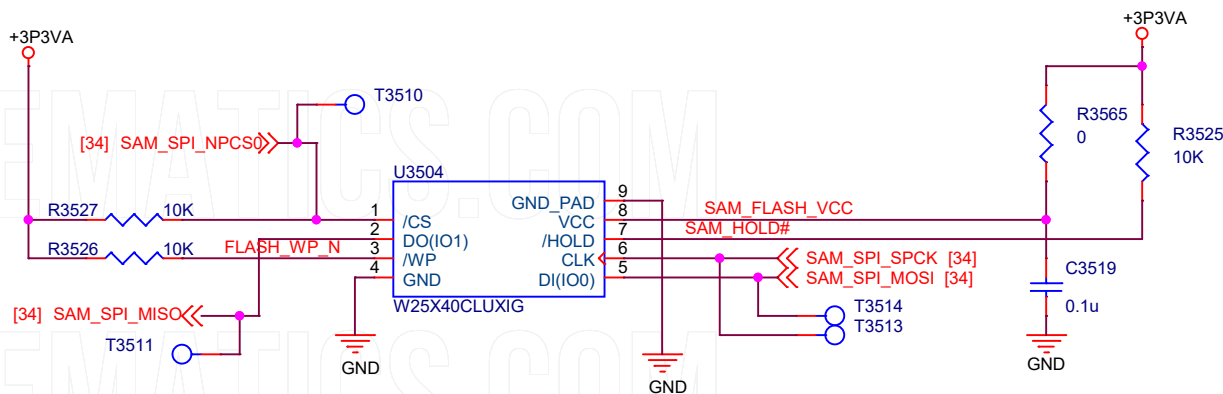
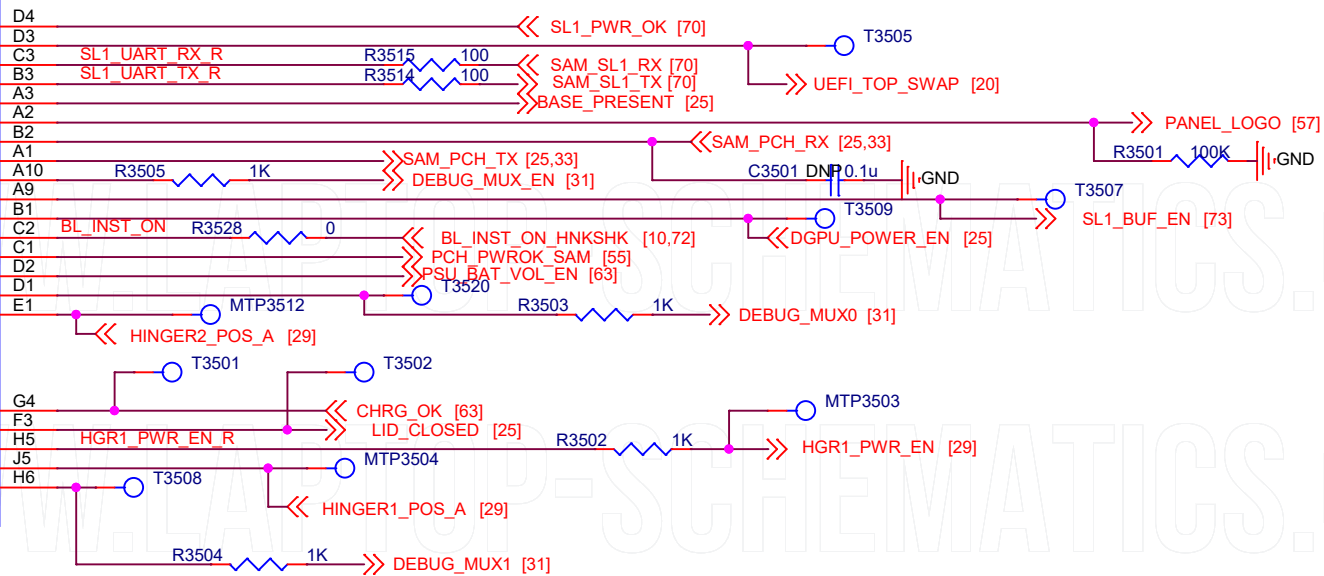
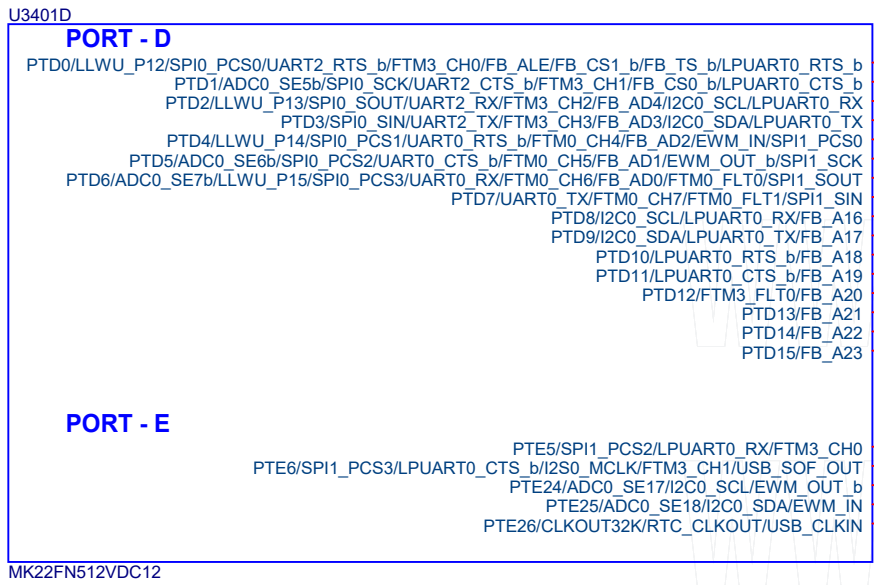


DEBUG CONN

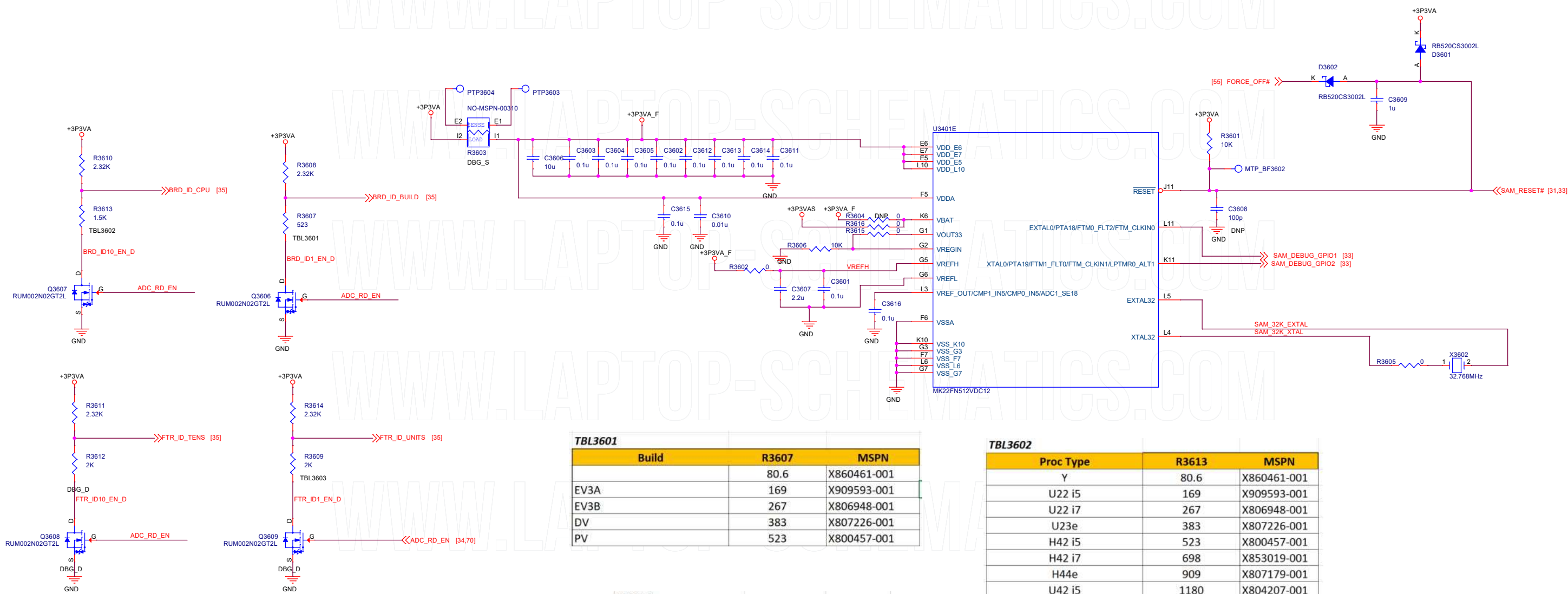


<Core Design>





	HINGER1_POS_A_R	HINGER1_POS_B_R
Closed	High	Low
Transition	High	High
Open	Low	High
fault	Low	Low

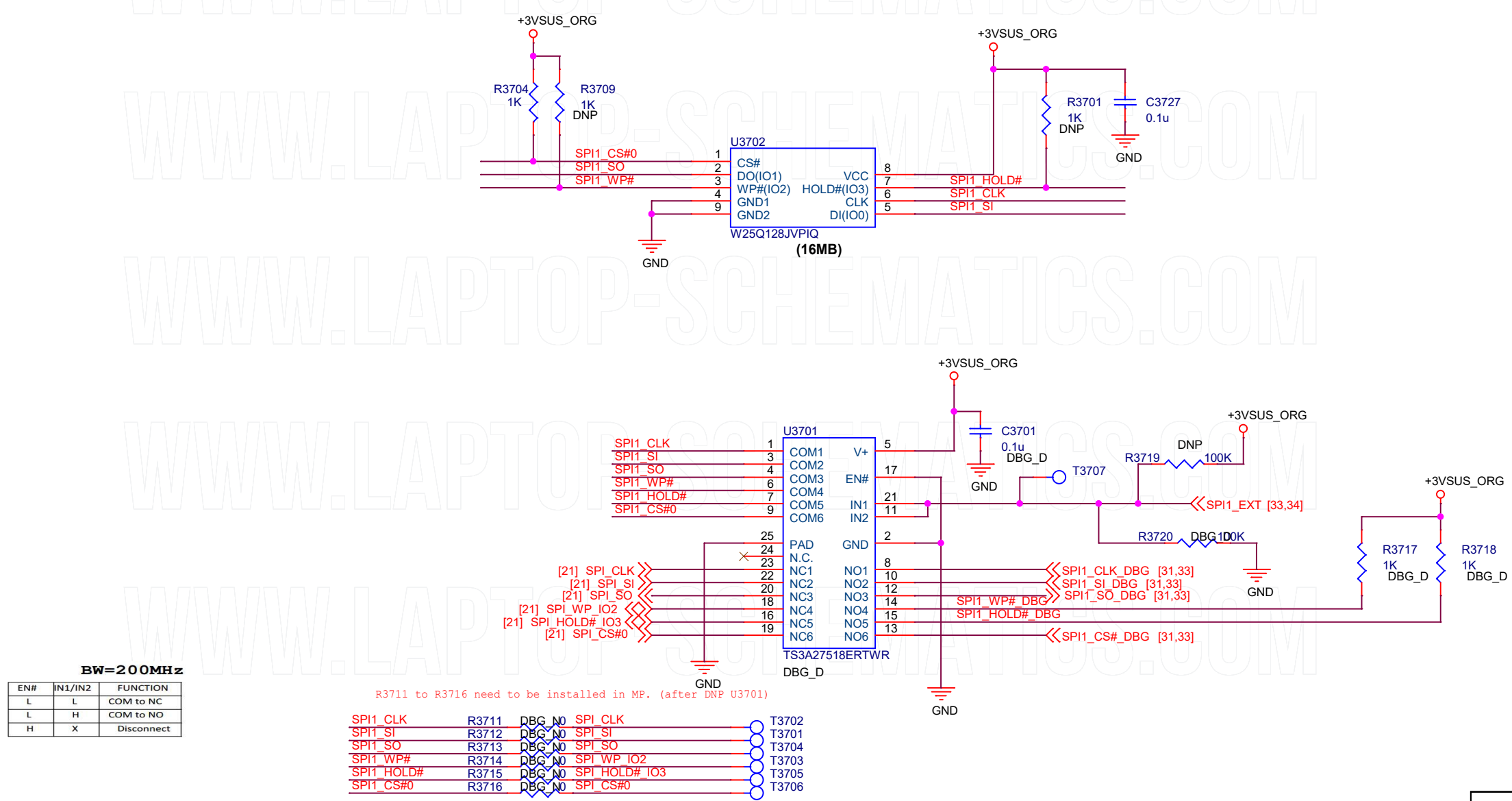


TBL3601		
Build	R3607	MSPN
EV3A	80.6	X860461-001
EV3B	169	X909593-001
DV	267	X806948-001
PV	383	X807226-001
	523	X800457-001

TBL3602		
Proc Type	R3613	MSPN
Y	80.6	X860461-001
U22 i5	169	X909593-001
U22 i7	267	X806948-001
U23e	383	X807226-001
H42 i5	523	X800457-001
H42 i7	698	X853019-001
H44e	909	X807179-001
U42 i5	1180	X804207-001
U42 i7	1500	X806696-001

TBL3603		
Build	R3609	MSPN
Gauntlet	1500	X806696-001
Shield	2000	X800427-001

DGPU\_PRESENT. Driven by SAM. This will indicate the presence of dGPU (1) or not (0).  
DGPU\_POWER\_STATE. Driven by SAM. This will indicate that the dGPU is powered up (1) or not (0). DGPU\_POWER\_STATE is always 0 when DGPU\_PRESENT is 0.  
DGPU\_POWER\_EN. Driven by PCH. This will request dGPU power to be turned on (1) or off (0). DGPU\_POWER\_EN is always 0 when DGPU\_PRESENT is 0



**BW=200MHz**

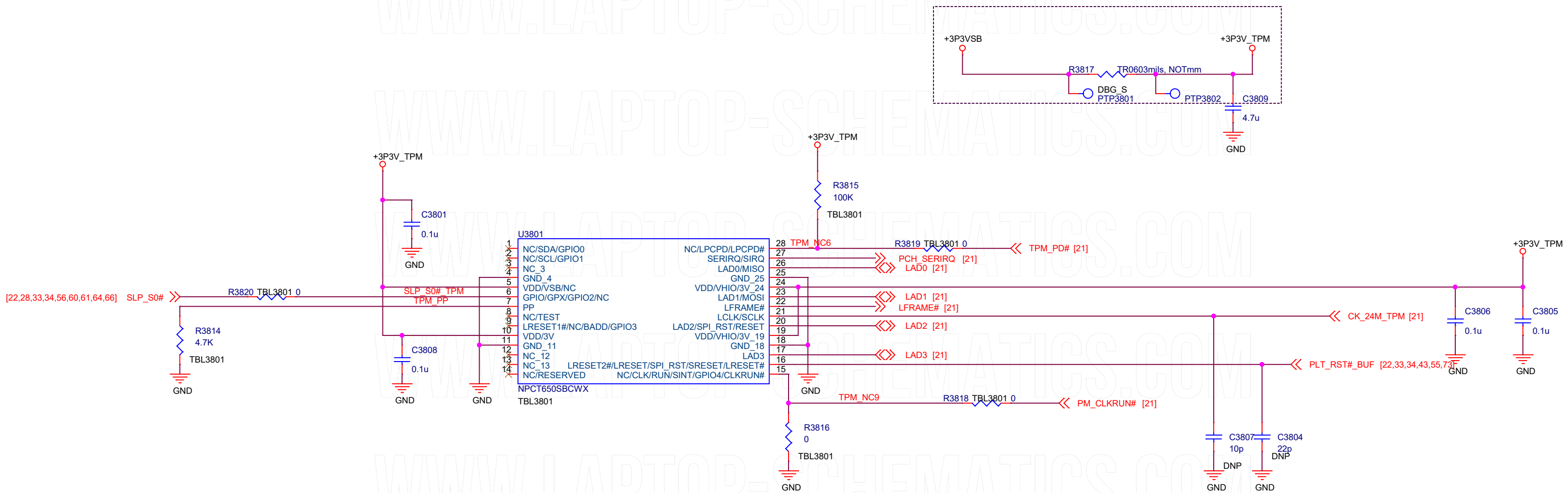
EN#	IN1/IN2	FUNCTION
L	L	COM to NC
L	H	COM to NO
H	X	Disconnect

R3711 to R3716 need to be installed in MP. (after DNP U3701)

SPI1_CLK	R3711	DBG_NO	SPI1_CLK	T3702
SPI1_SI	R3712	DBG_NO	SPI1_SI	T3701
SPI1_SO	R3713	DBG_NO	SPI1_SO	T3704
SPI1_WP#	R3714	DBG_NO	SPI1_WP# IO2	T3703
SPI1_HOLD#	R3715	DBG_NO	SPI1_HOLD# IO3	T3705
SPI1_CS#0	R3716	DBG_NO	SPI1_CS#0	T3706



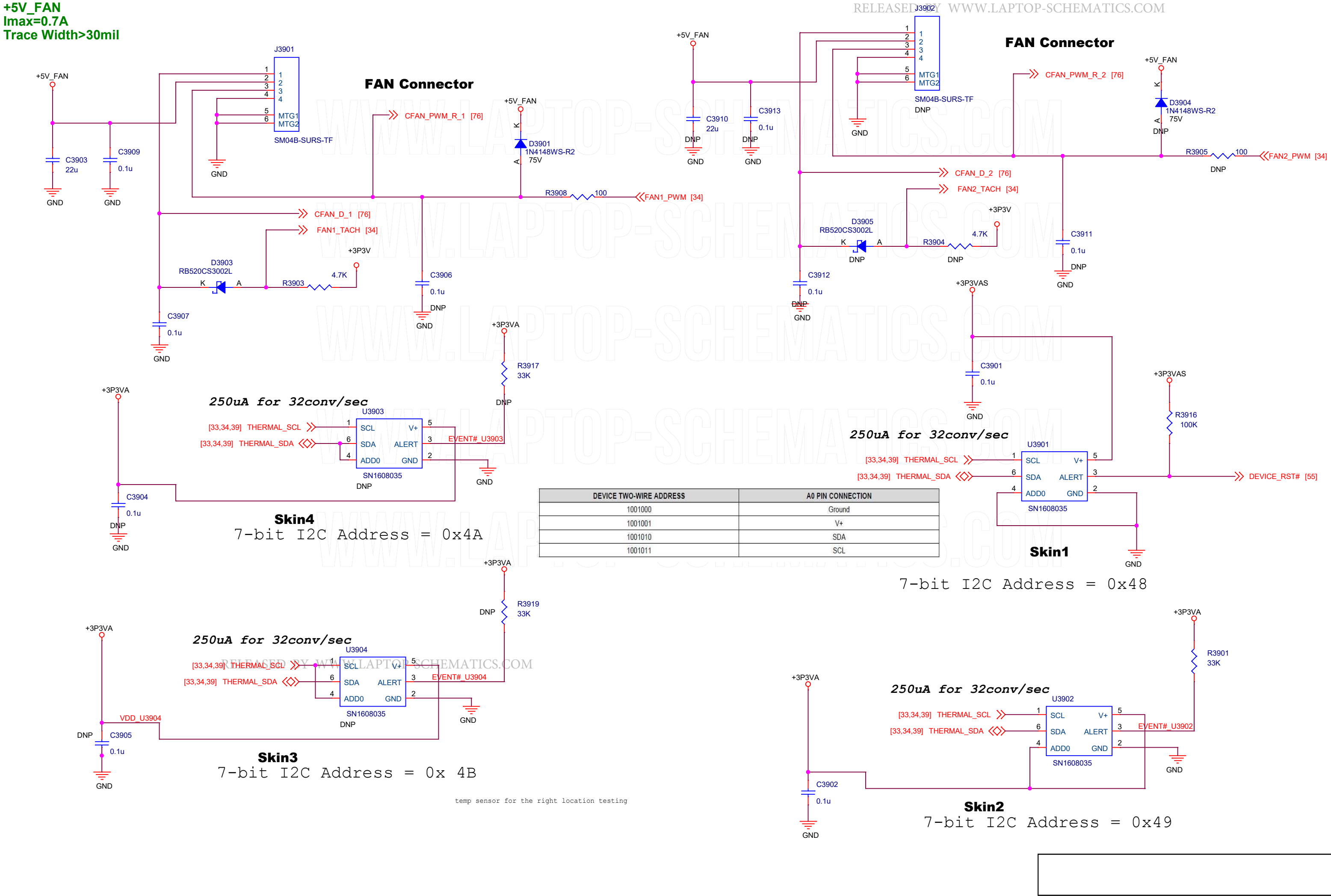
# Trusted Platform Module



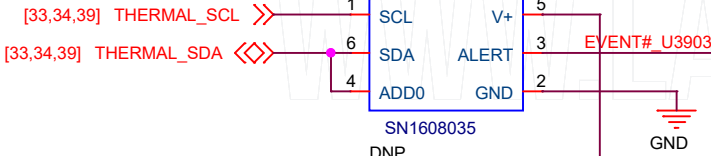
NationZ Z32H320TC do not support CLKRUN# and LPCPD# function  
IFX don't have PP funcnation in TPM2.0

TBL3801			
Ref	Infineon	NationZ	Nuvoton
R2701	X811791-001	NO-STUFF	X811791-001
R2703	NO-STUFF	X811791-001	NO-STUFF
R3814	X852314-001	NO-STUFF	X852314-001
R3815	NO-STUFF	X813010-001	NO-STUFF
R3816	NO-STUFF	X811786-001	NO-STUFF
R3818	NO-STUFF	NO-STUFF	X811786-001
R3819	NO-STUFF	NO-STUFF	X811786-001
R3820	NO-STUFF	NO-STUFF	X811786-001
U3801	X912460-002	X930840-002	M1006791-003

+5V\_FAN  
Imax=0.7A  
Trace Width>30mil

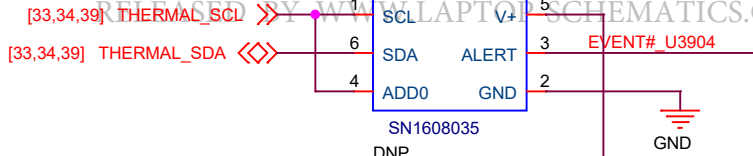


250uA for 32conv/sec



**Skin4**  
7-bit I2C Address = 0x4A

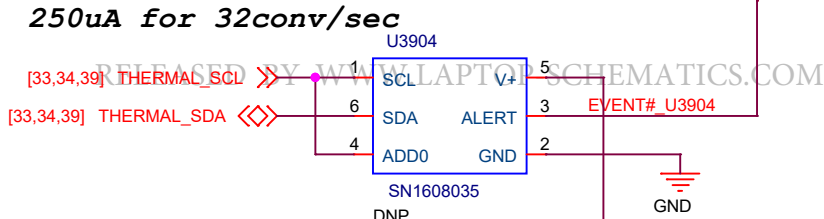
250uA for 32conv/sec



7-bit I2C Address = 0x48

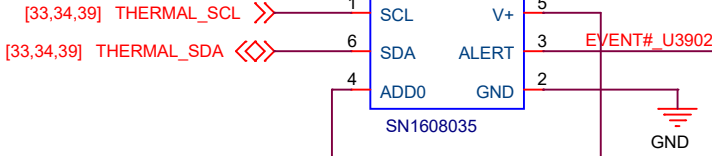
**Skin3**

7-bit I2C Address = 0x 4B



temp sensor for the right location testing

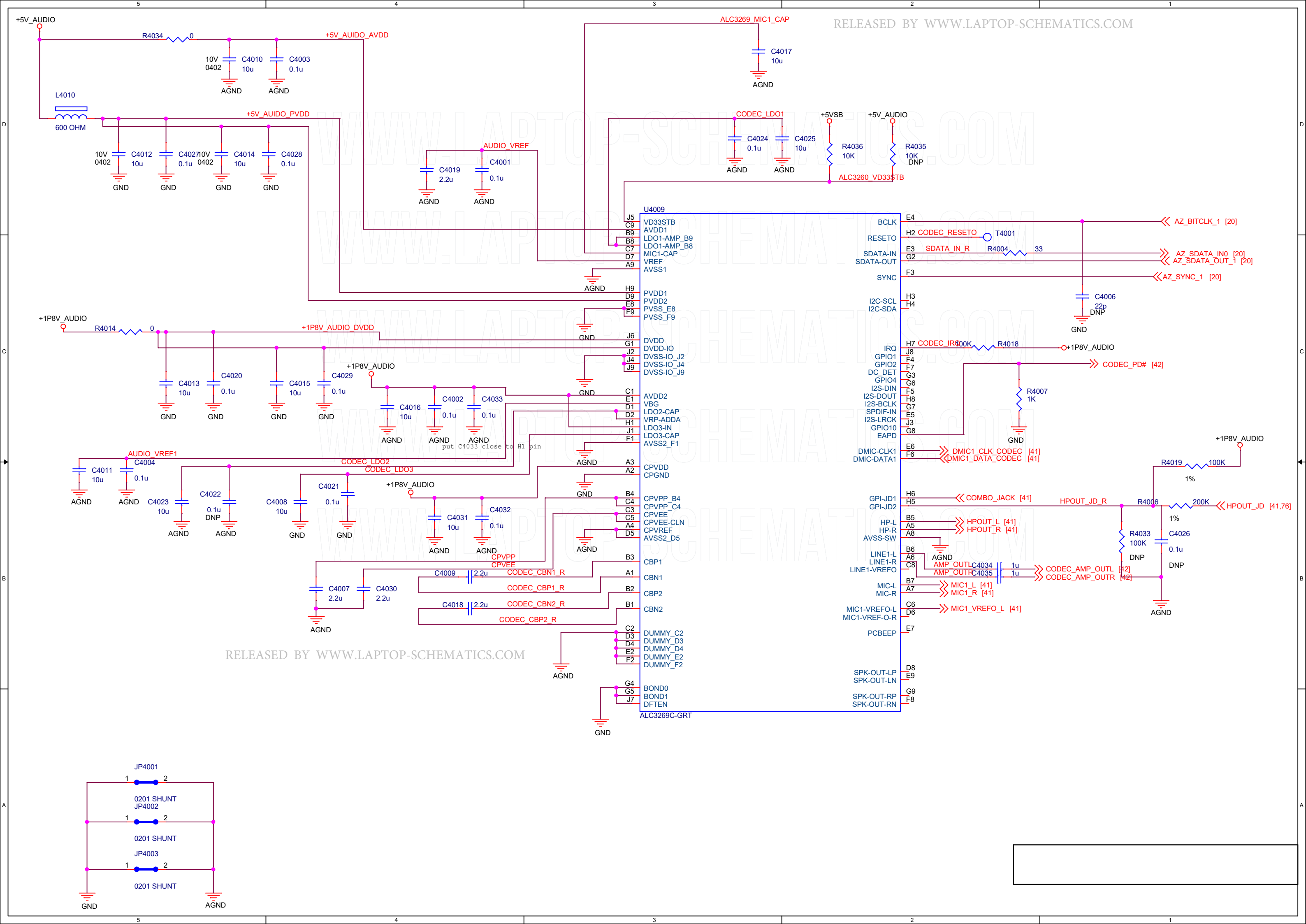
250uA for 32conv/sec



**Skin2**

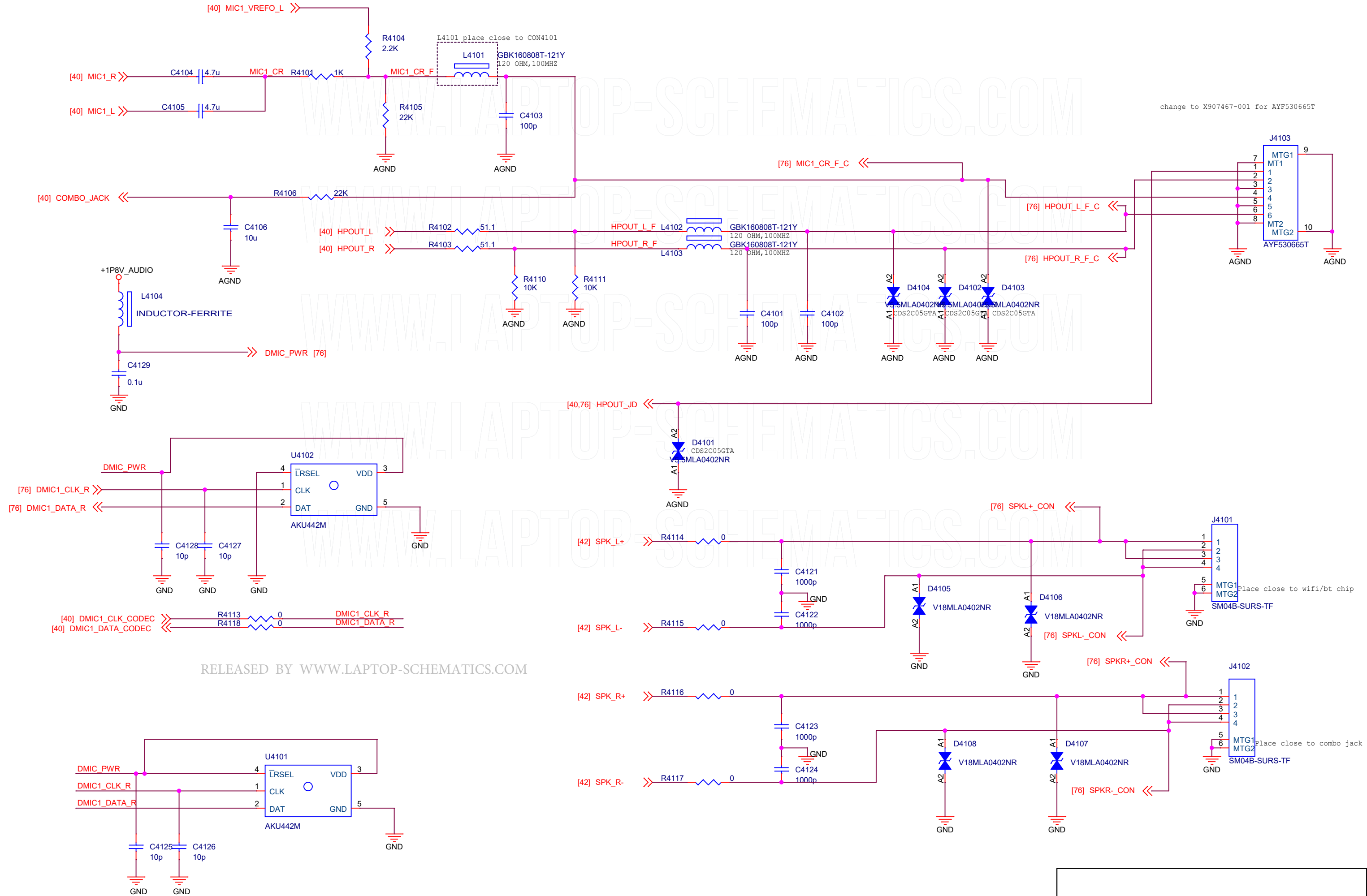
7-bit I2C Address = 0x49





# HP/MIC1 Combo Jack

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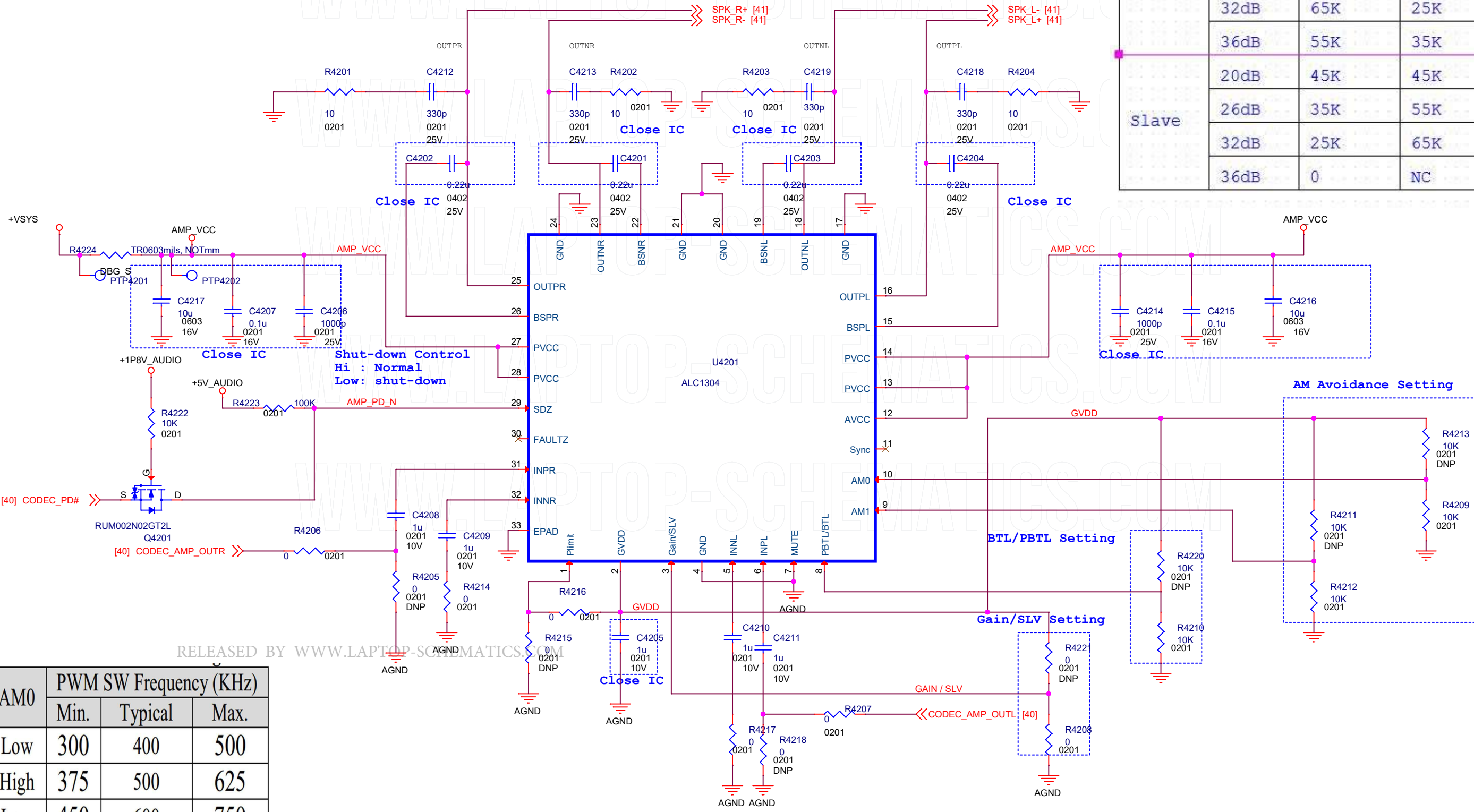




Stereo Input (S.E.)  
Stereo Output-BTL

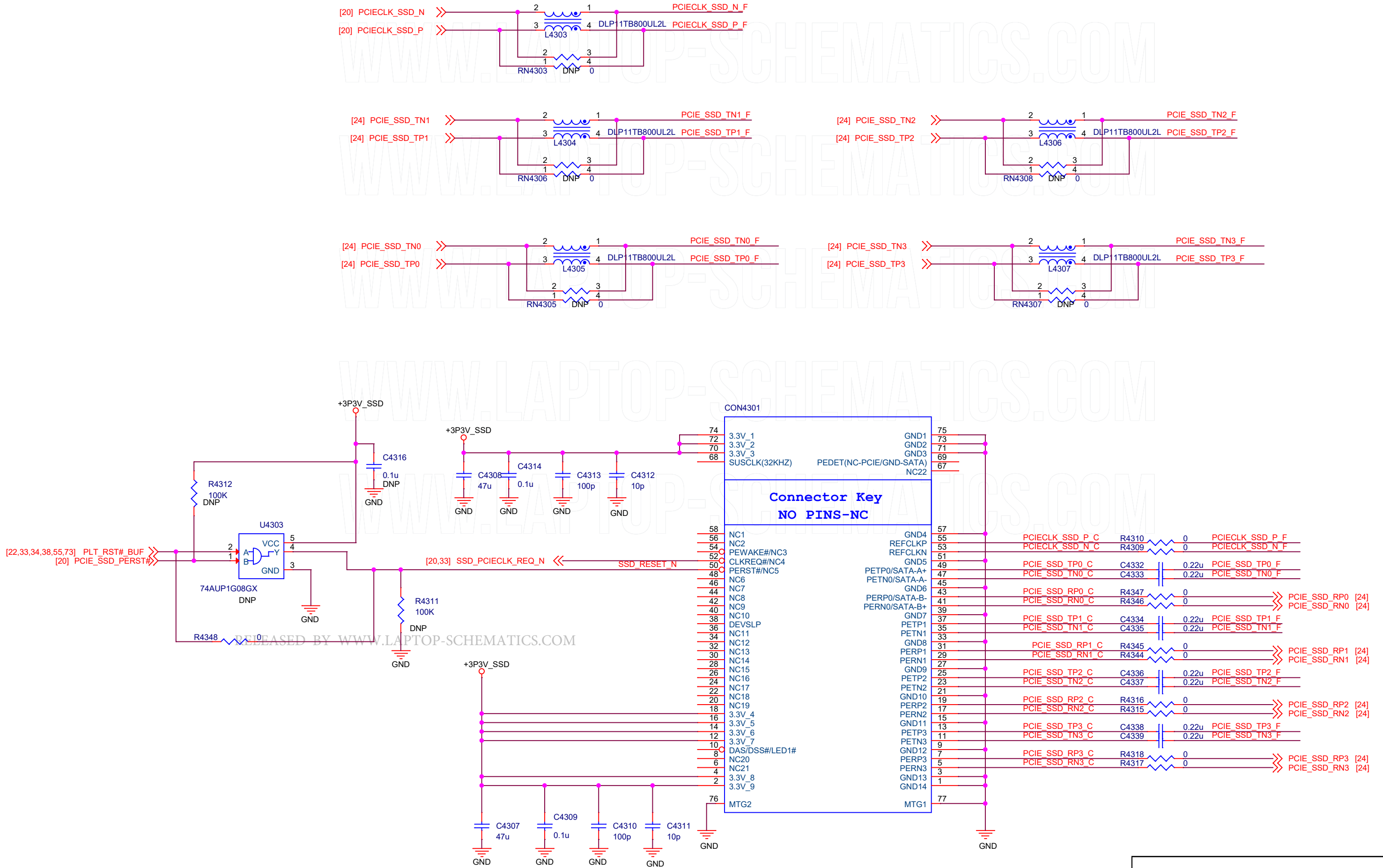
**SPKR Trace Width**  
1. Maximum trace resistance for each channel less than 0.5 ohms.  
2. Each of 4 traces, measured from CODEC to speaker connector, less than 0.25 ohms

		R4221	R4208
Mode	Gain	RX (ohm)	RY (ohm)
Master	20dB	NC	0
	26dB	75K	15K
	32dB	65K	25K
	36dB	55K	35K
Slave	20dB	45K	45K
	26dB	35K	55K
	32dB	25K	65K
	36dB	0	NC

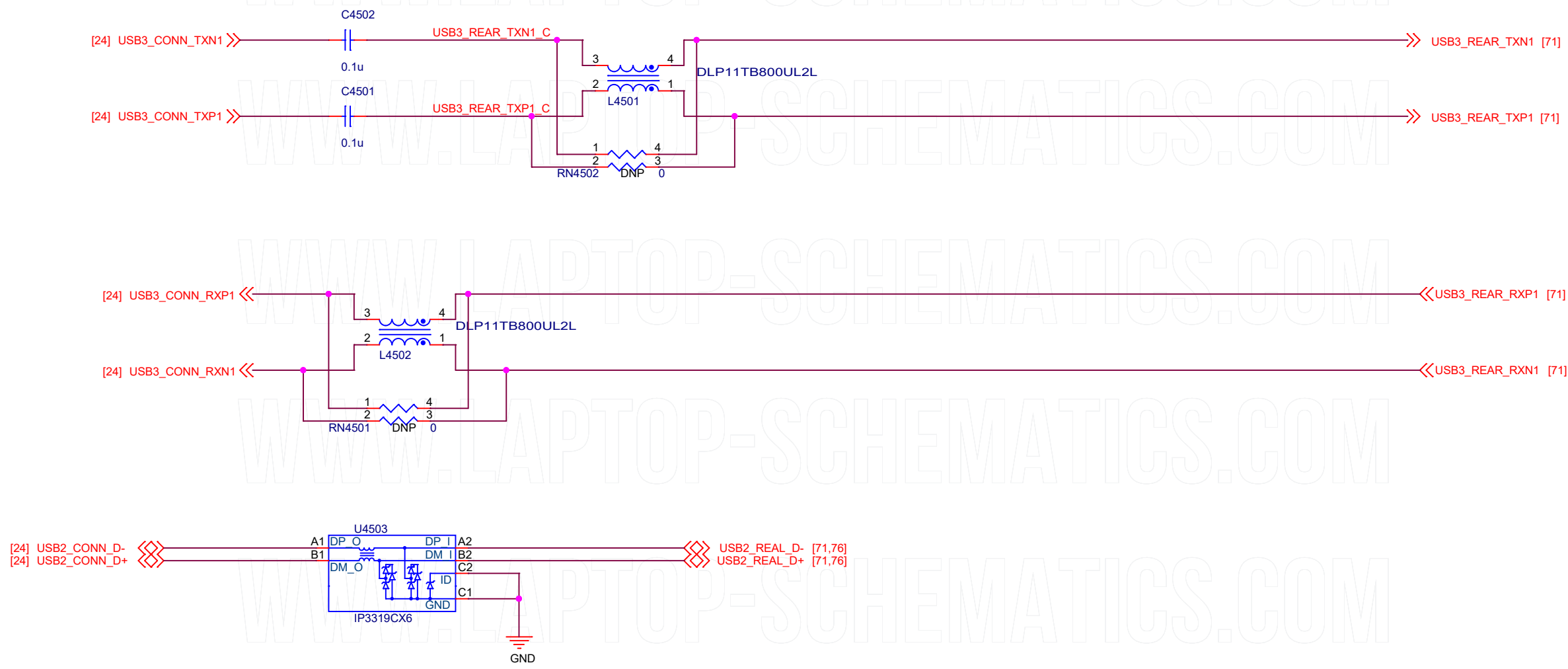


AM1	AM0	PWM SW Frequency (KHz)		
		Min.	Typical	Max.
Low	Low	300	400	500
Low	High	375	500	625
High	Low	450	600	750
High	High	750	1000	1250









Note: IP3319CX6 D+ and D- is interchangeable as seen in data sheet. Flipped for layout convenience.

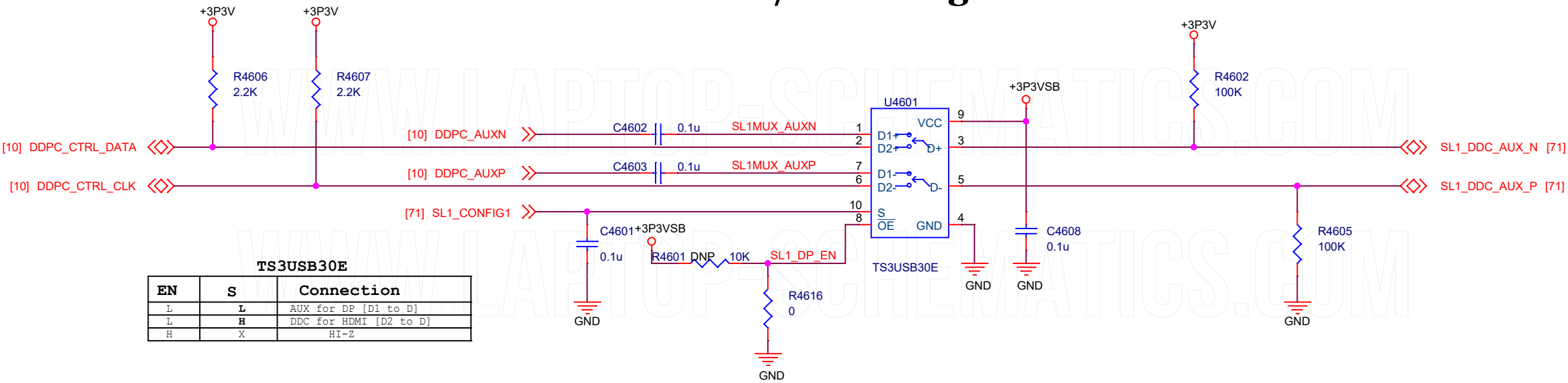
WWW.LAPTOP-SCHEMATICS.COM

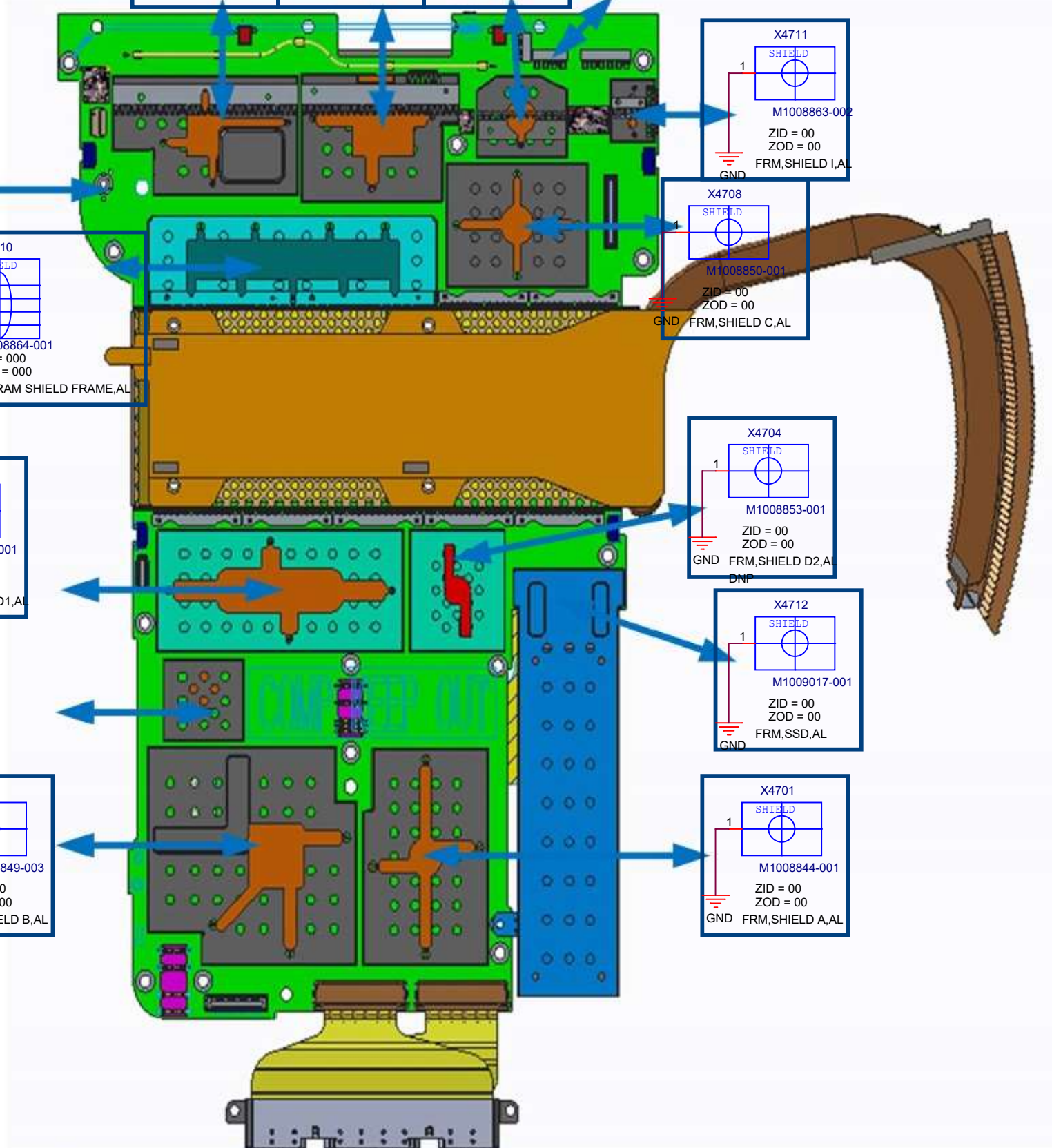
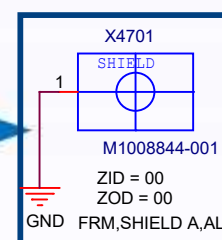
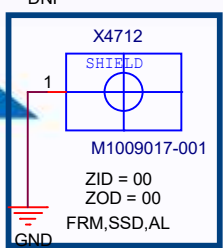
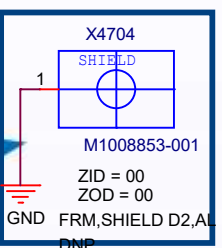
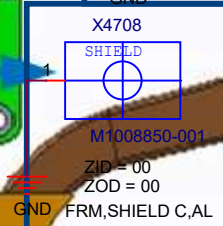
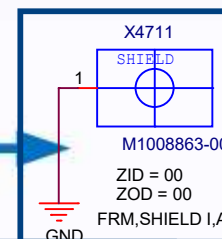
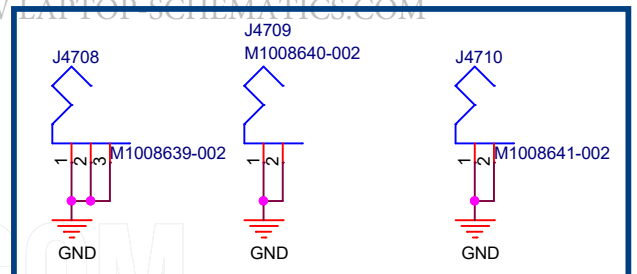
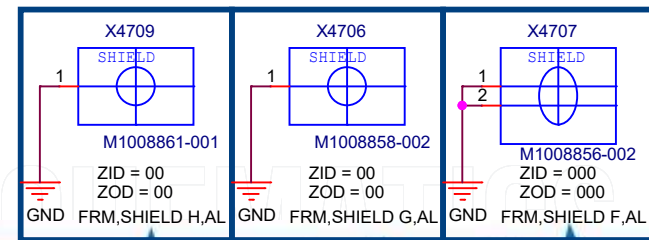
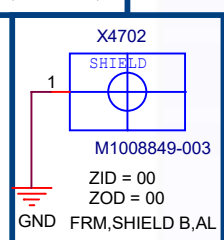
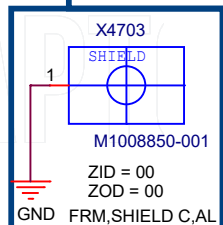
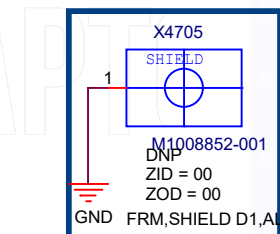
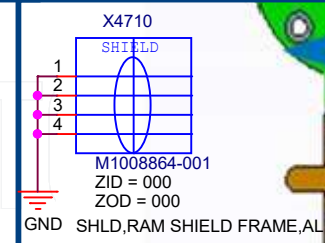
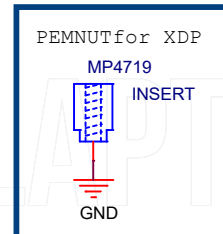
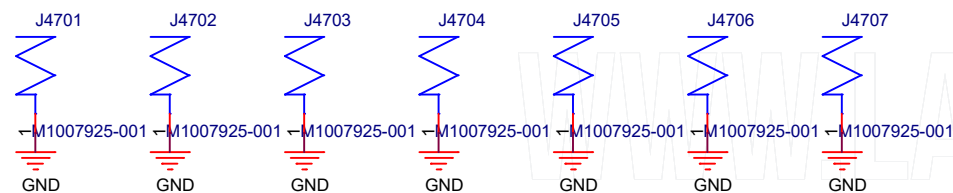
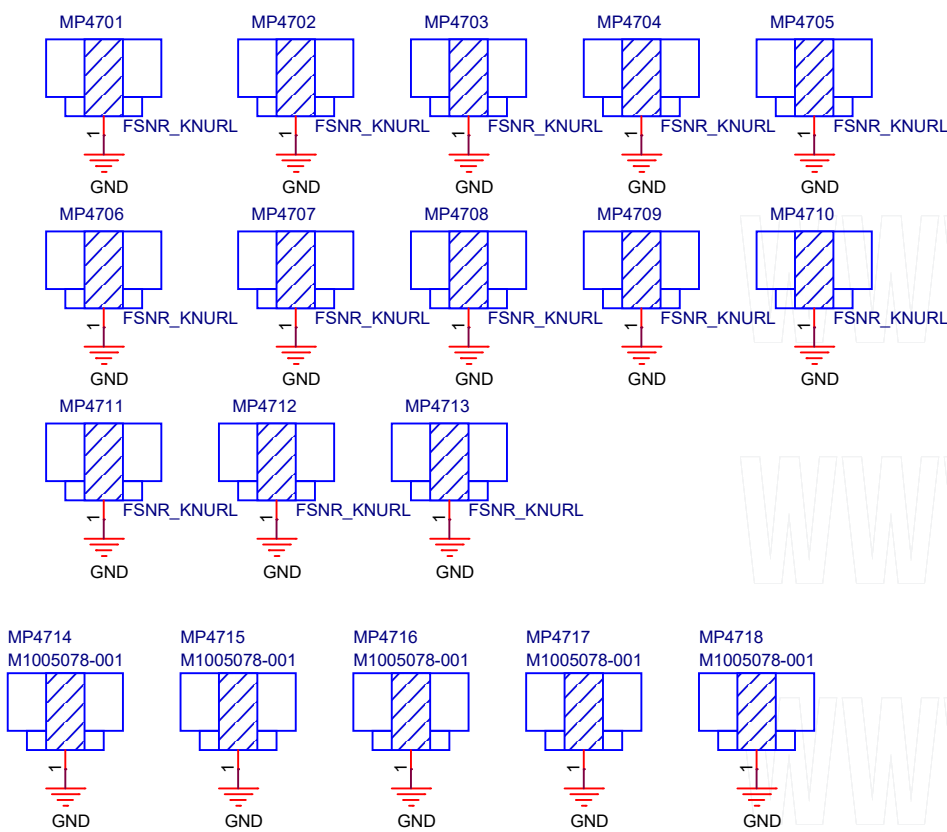
WWW.LAPTOP-SCHEMATICS.COM

when you TI ts3usb30e (X870617-001), NIR4613 and R4601 and install R4615 and R4616

WWW.LAPTOP-SCHEMATICS.COM

SL1 DP mux to HDMI/DVI Dongle control



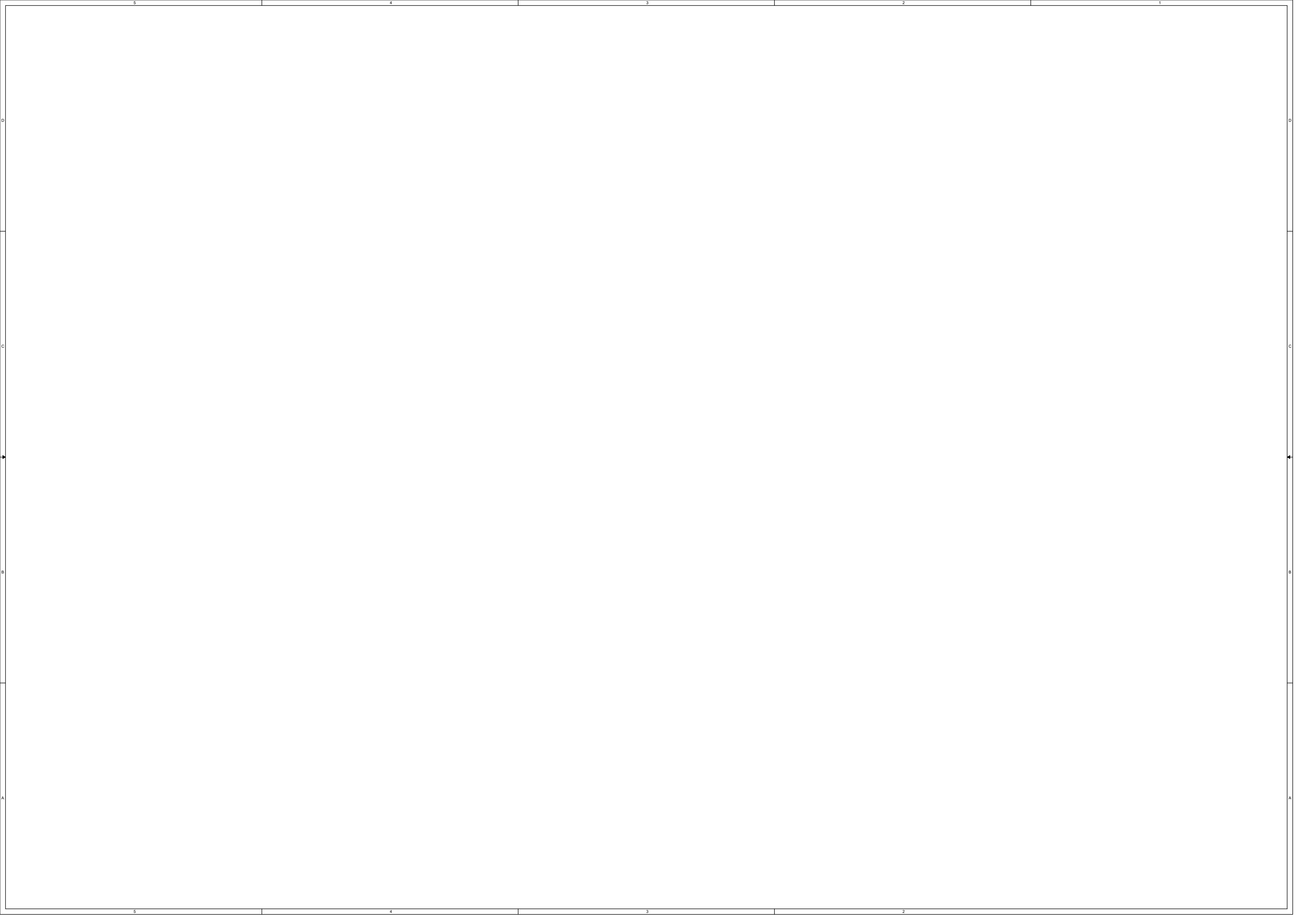




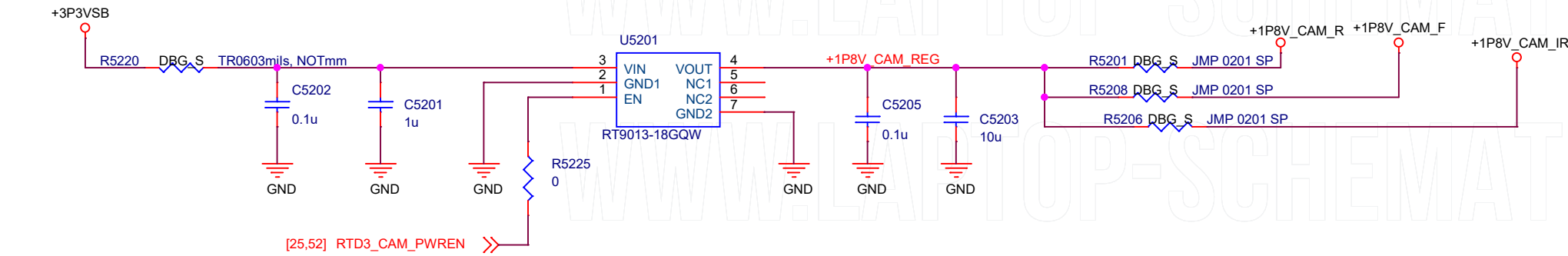




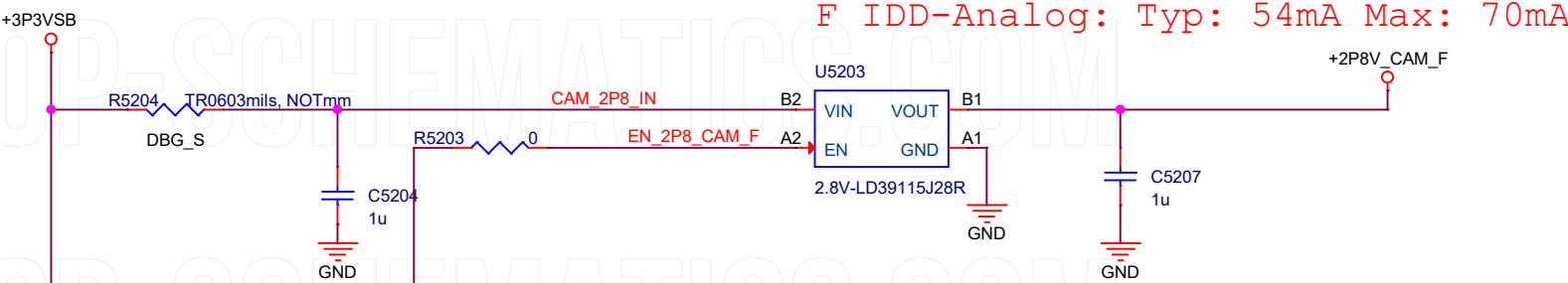




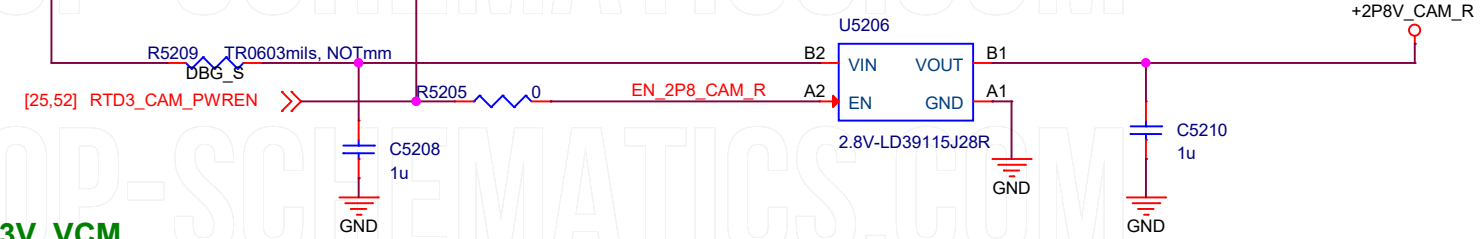
IR IDD-IO: Typ: 40mA Max: 55mA  
Front IDD-IO+Core: Typ: 67.5mA Max: 93mA  
Rear IDD-IO: Typ: 3.3mA Max: 4.5mA



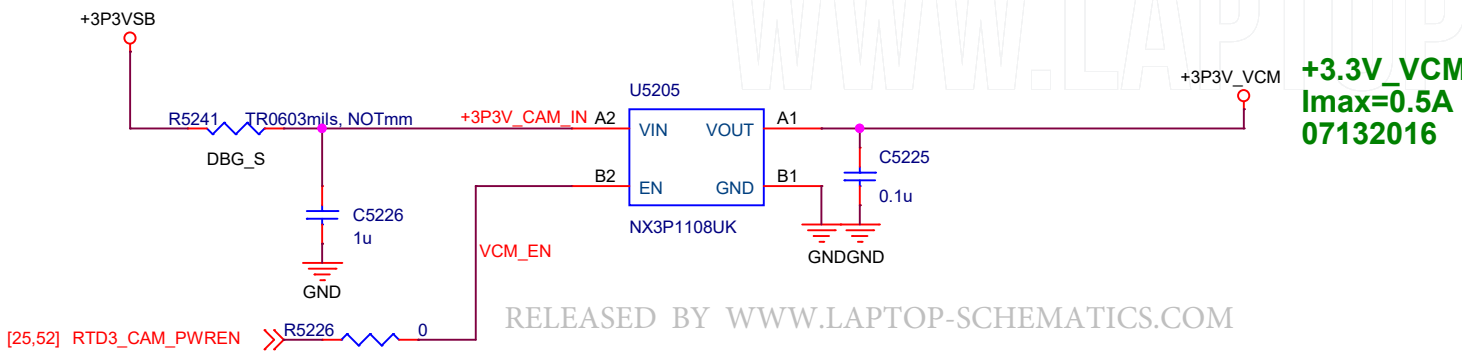
2V8\_LDO\_Voltage Regulator



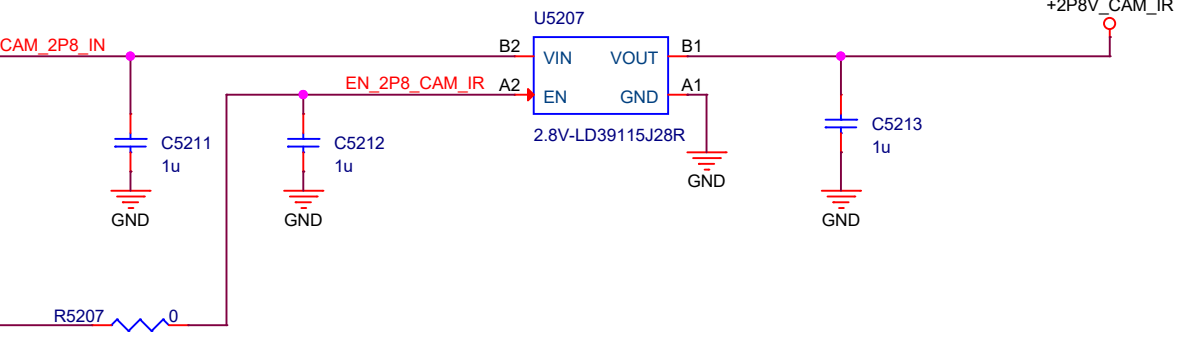
F IDD-Analog: Typ: 54mA Max: 70mA



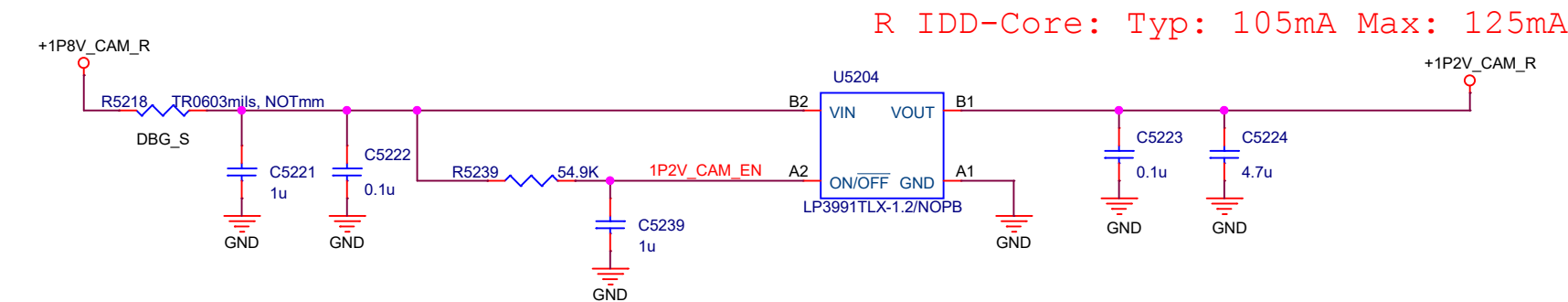
R IDD-Analog: Typ: 23mA Max: 30mA



+3.3V\_VCM  
Imax=0.5A  
07132016

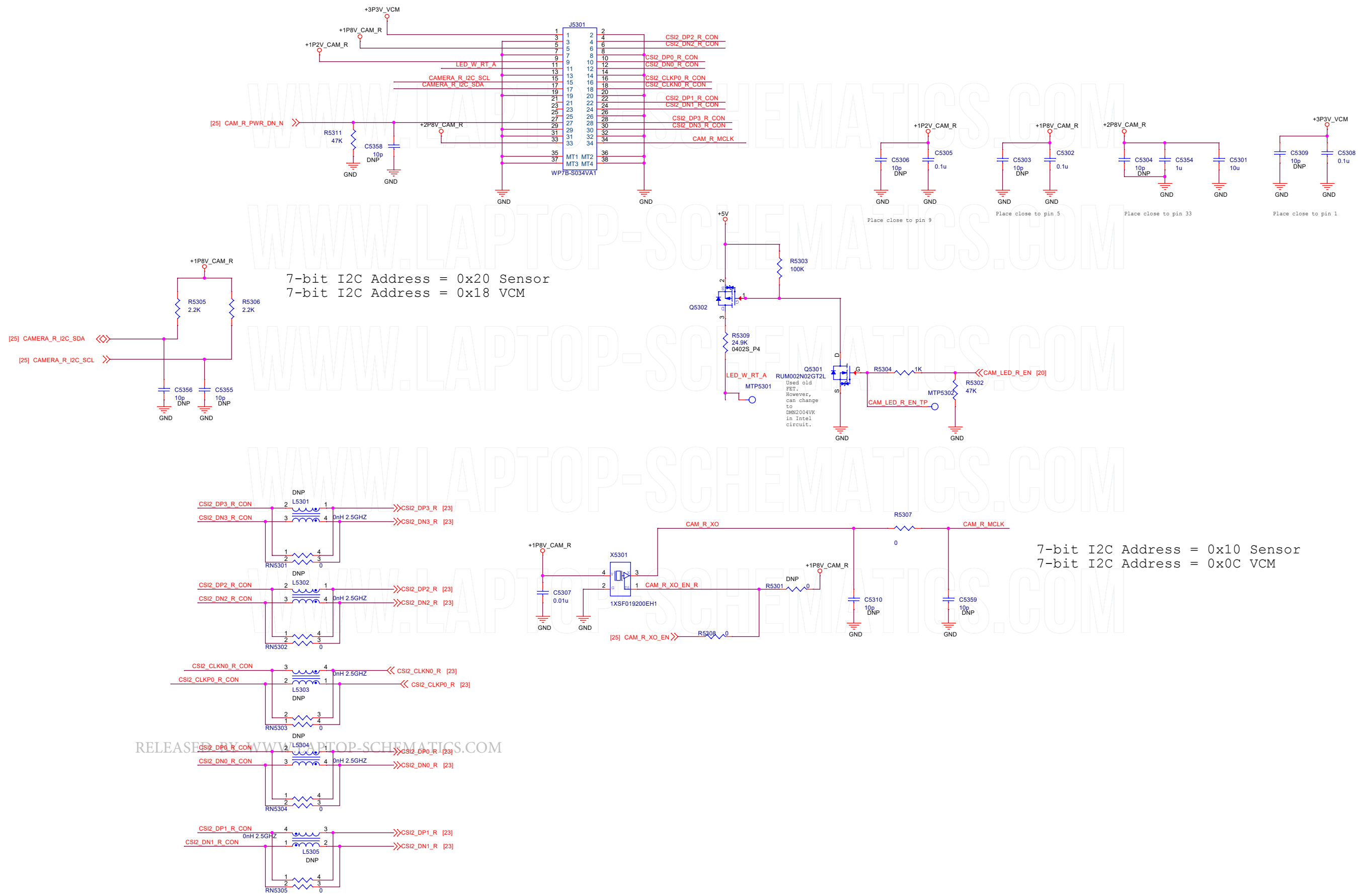


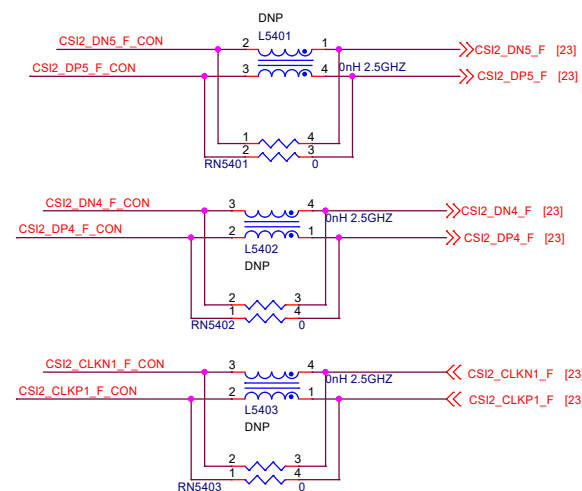
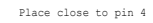
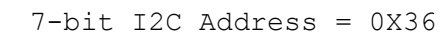
IR IDD-Analog: Typ: 16mA Max: 20mA

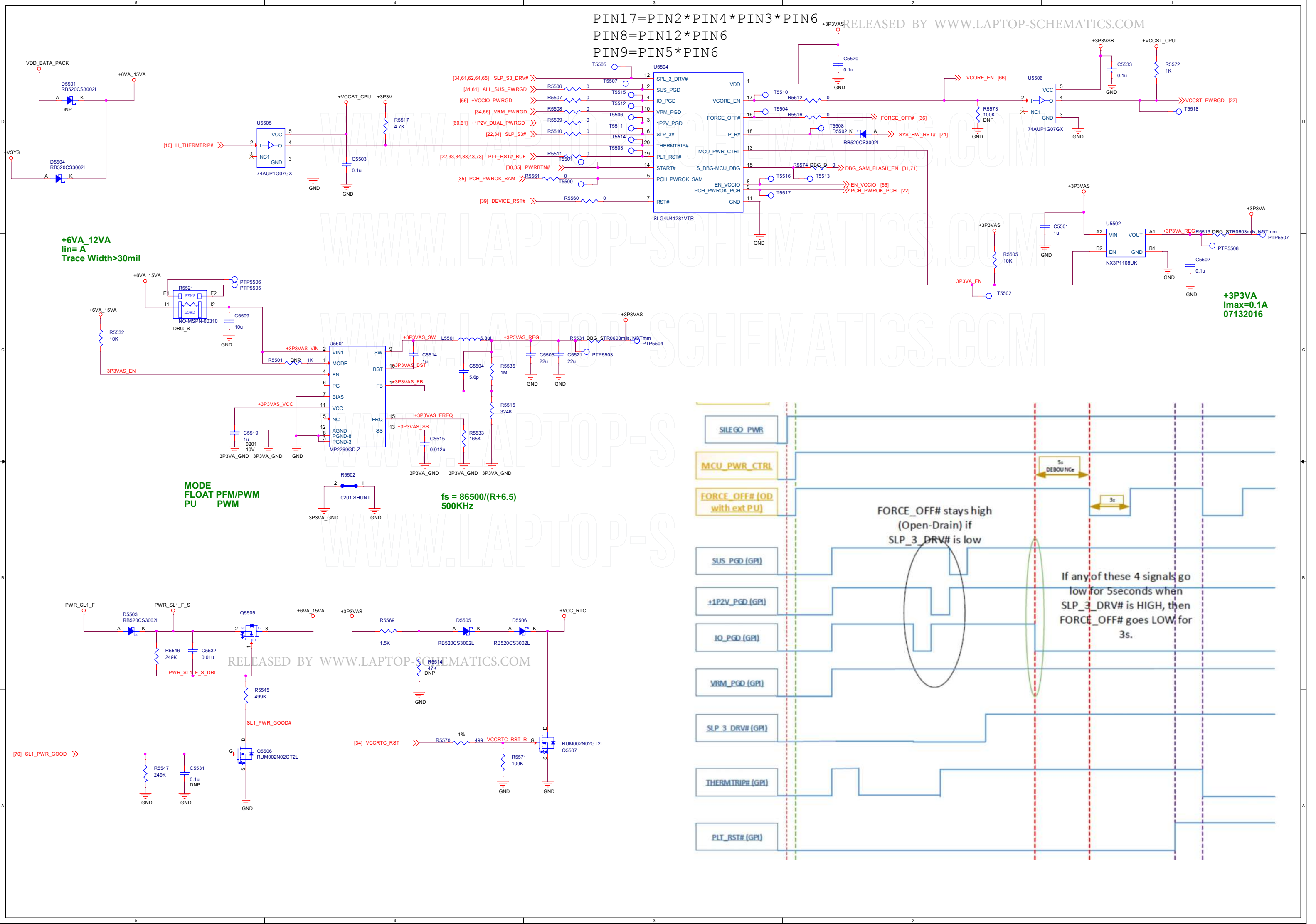


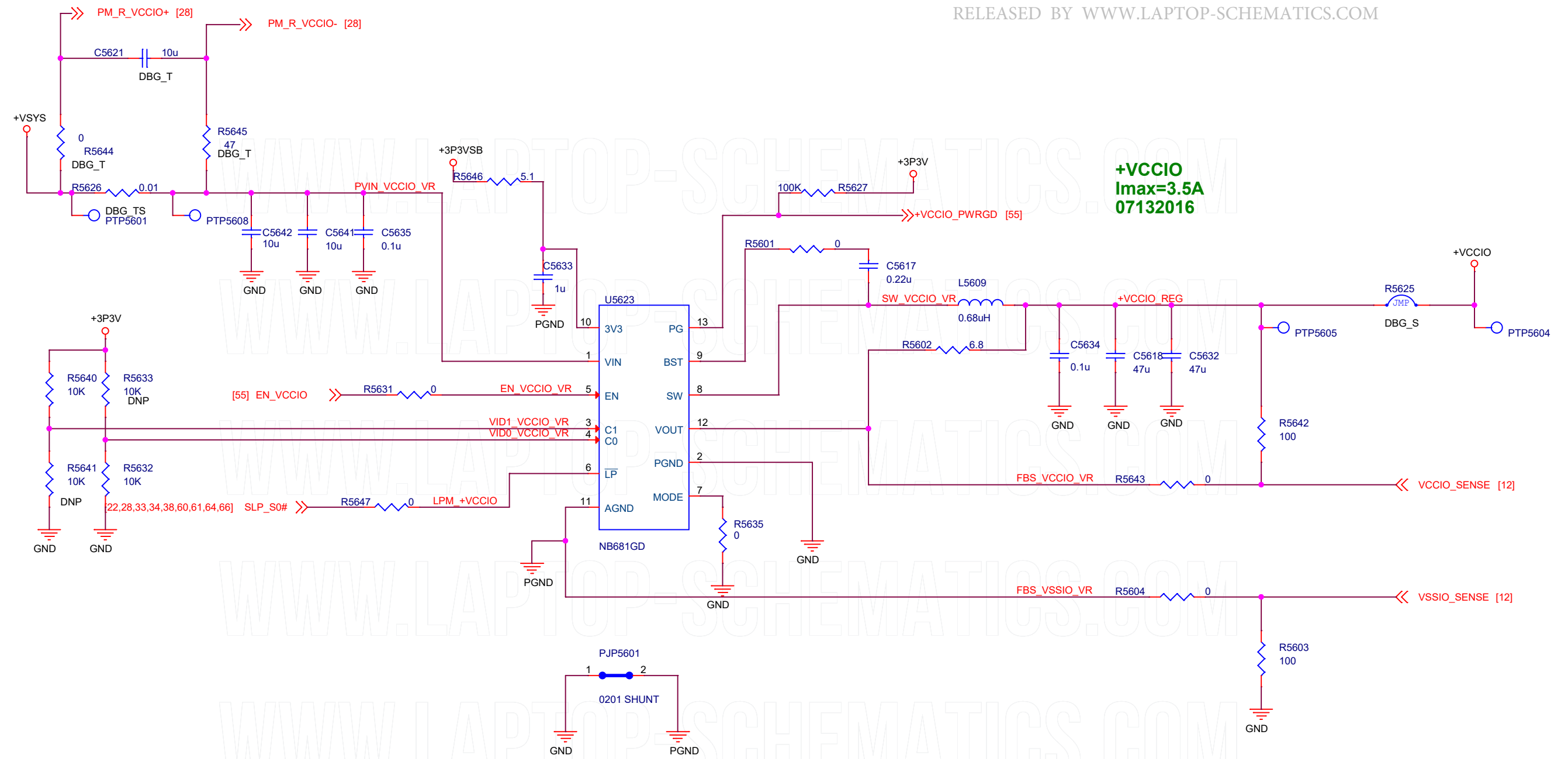
R IDD-Core: Typ: 105mA Max: 125mA

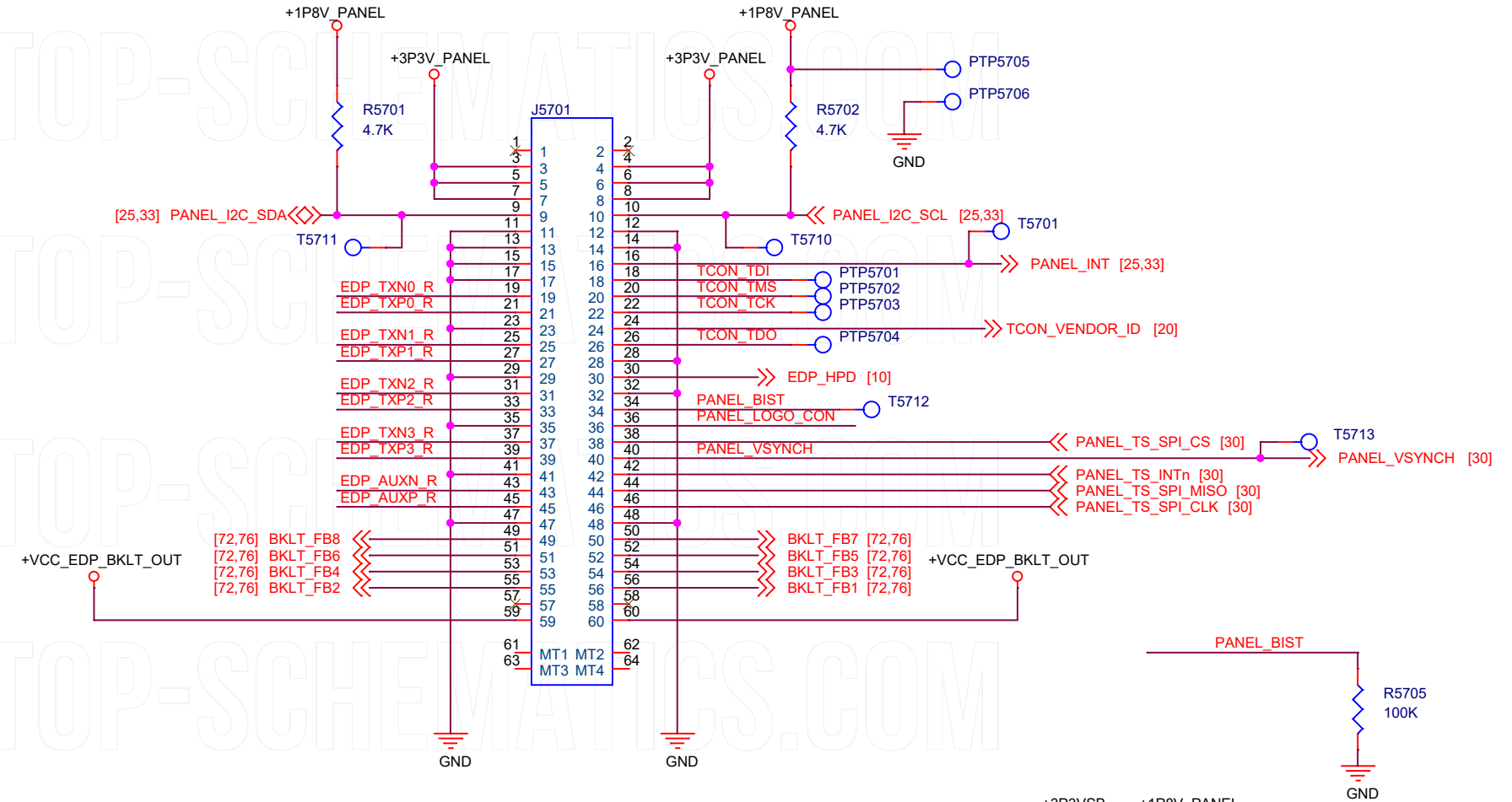
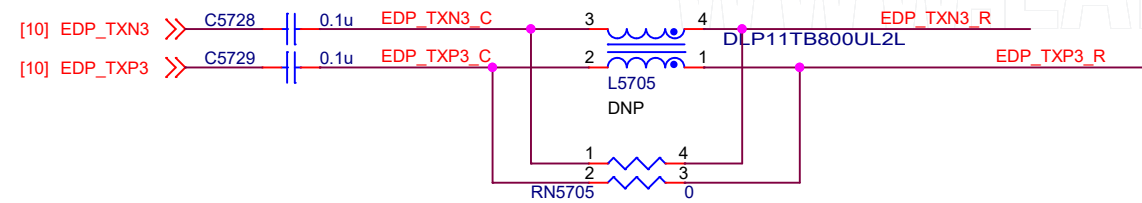
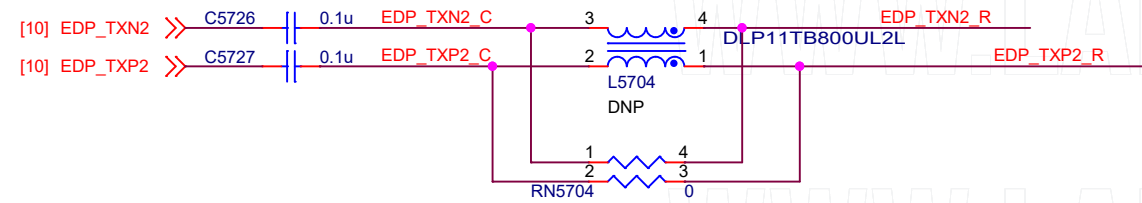
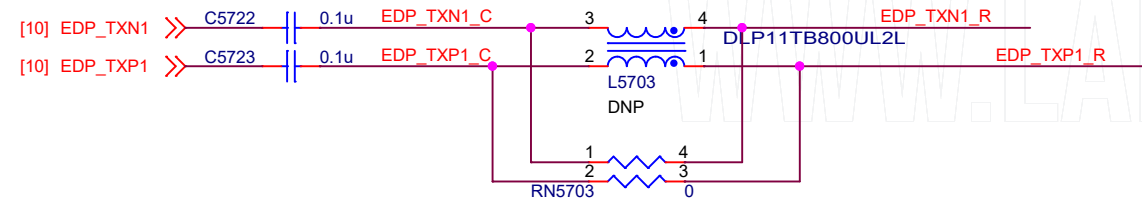
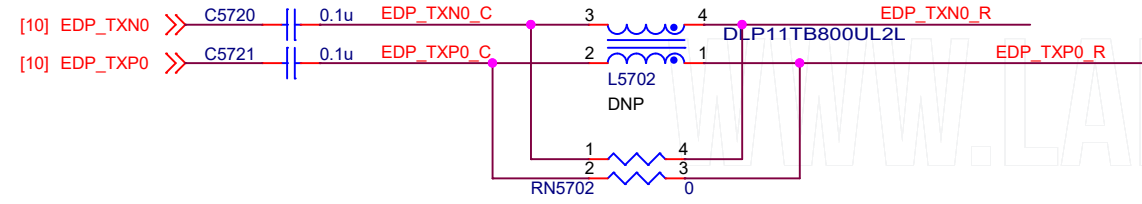
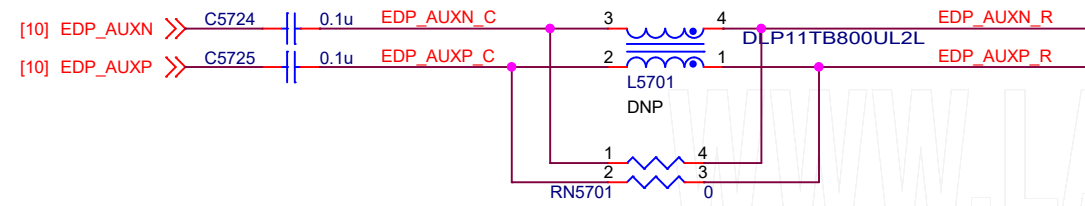




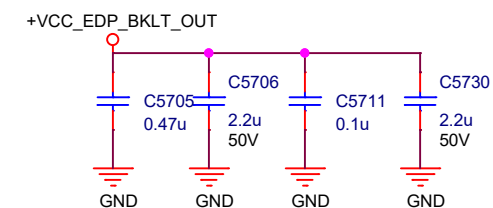
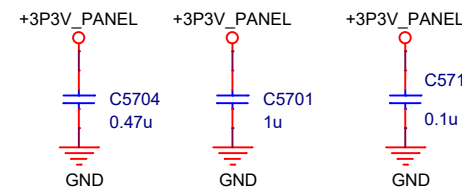
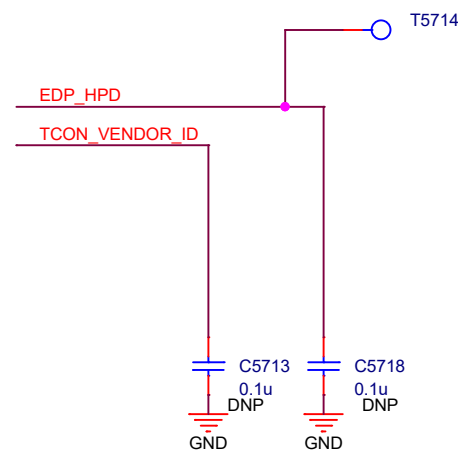
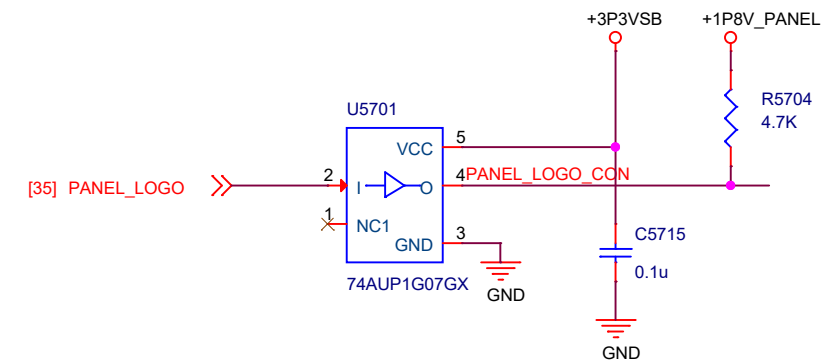




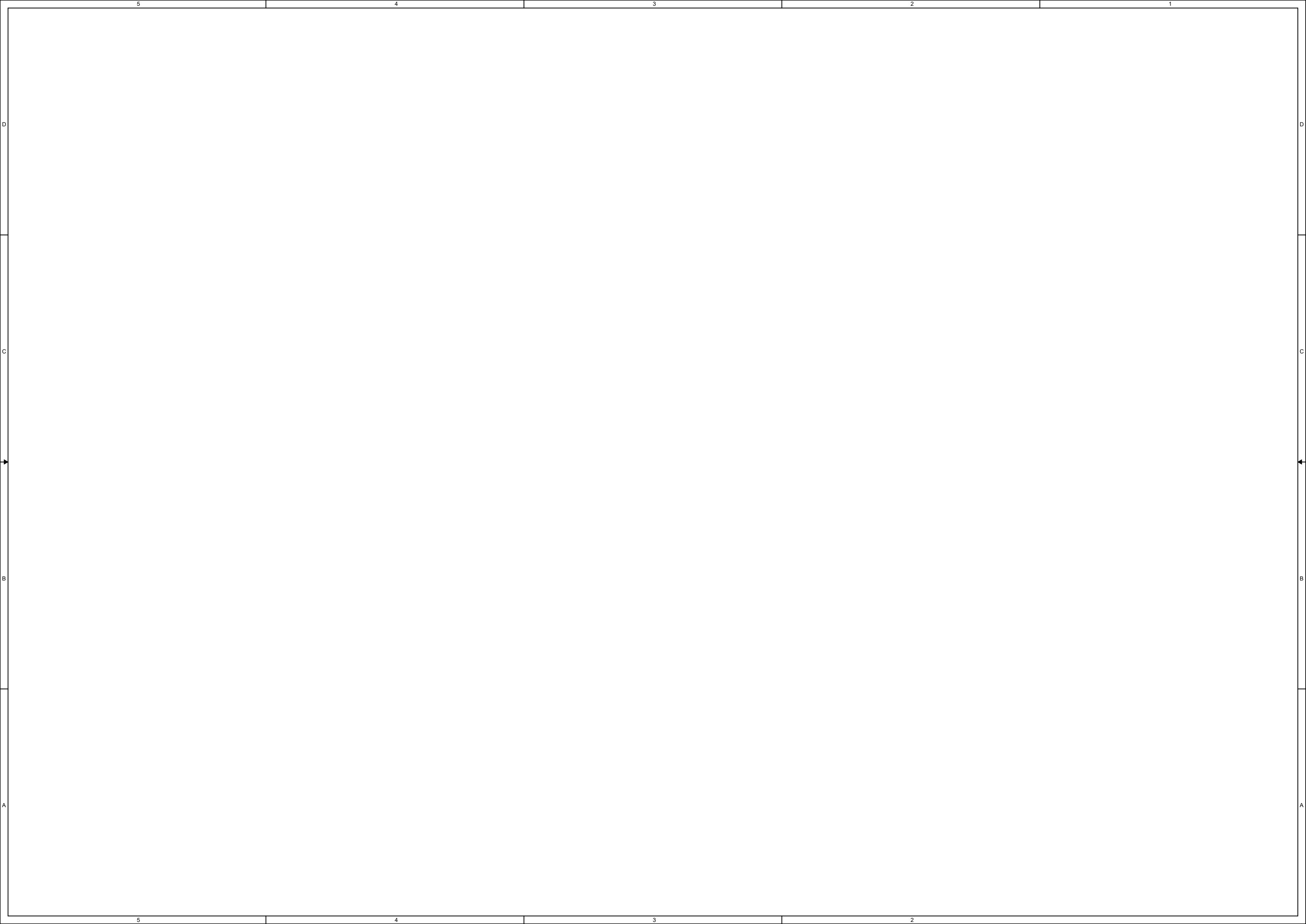


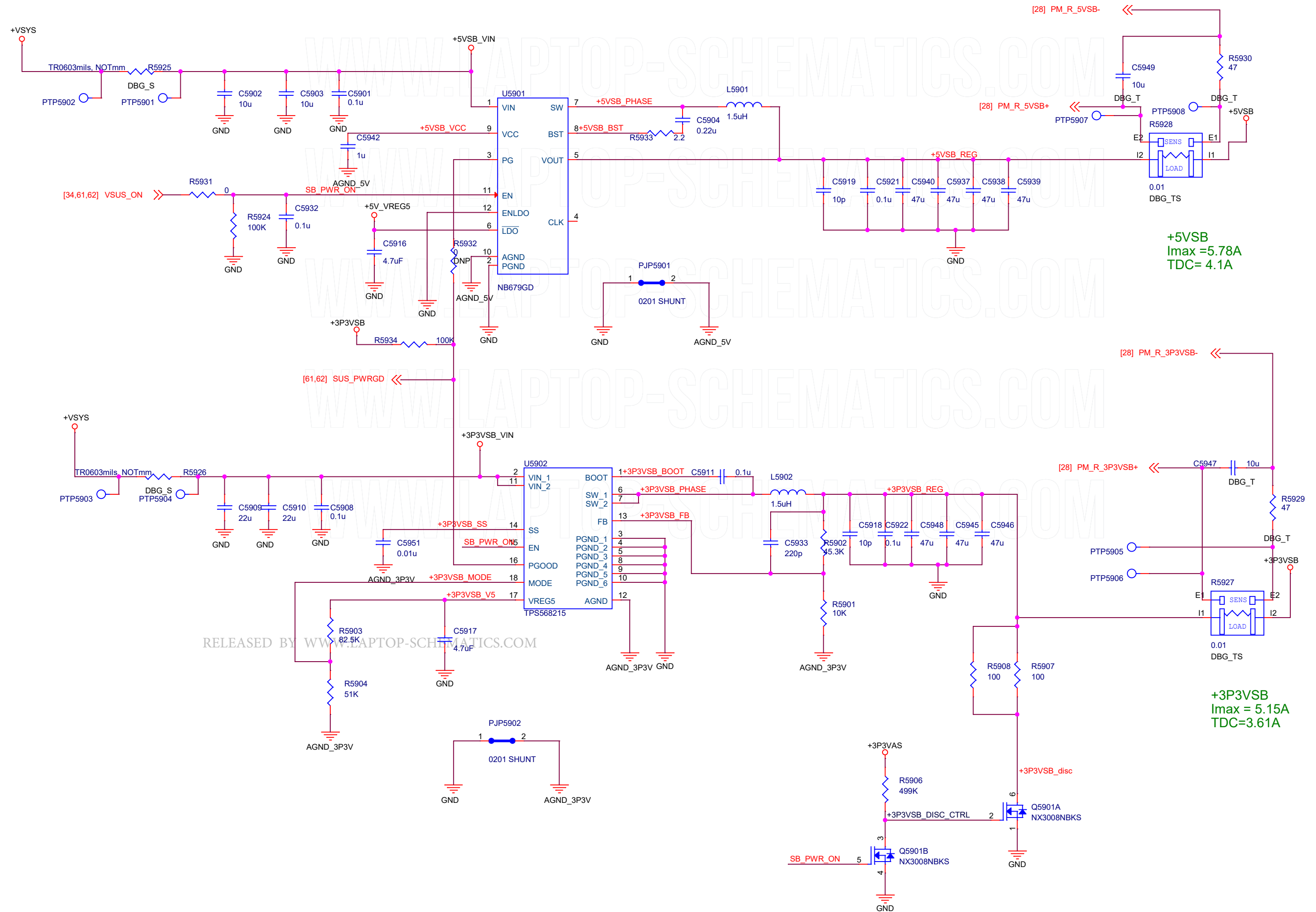


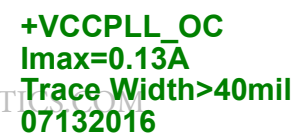
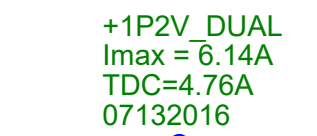
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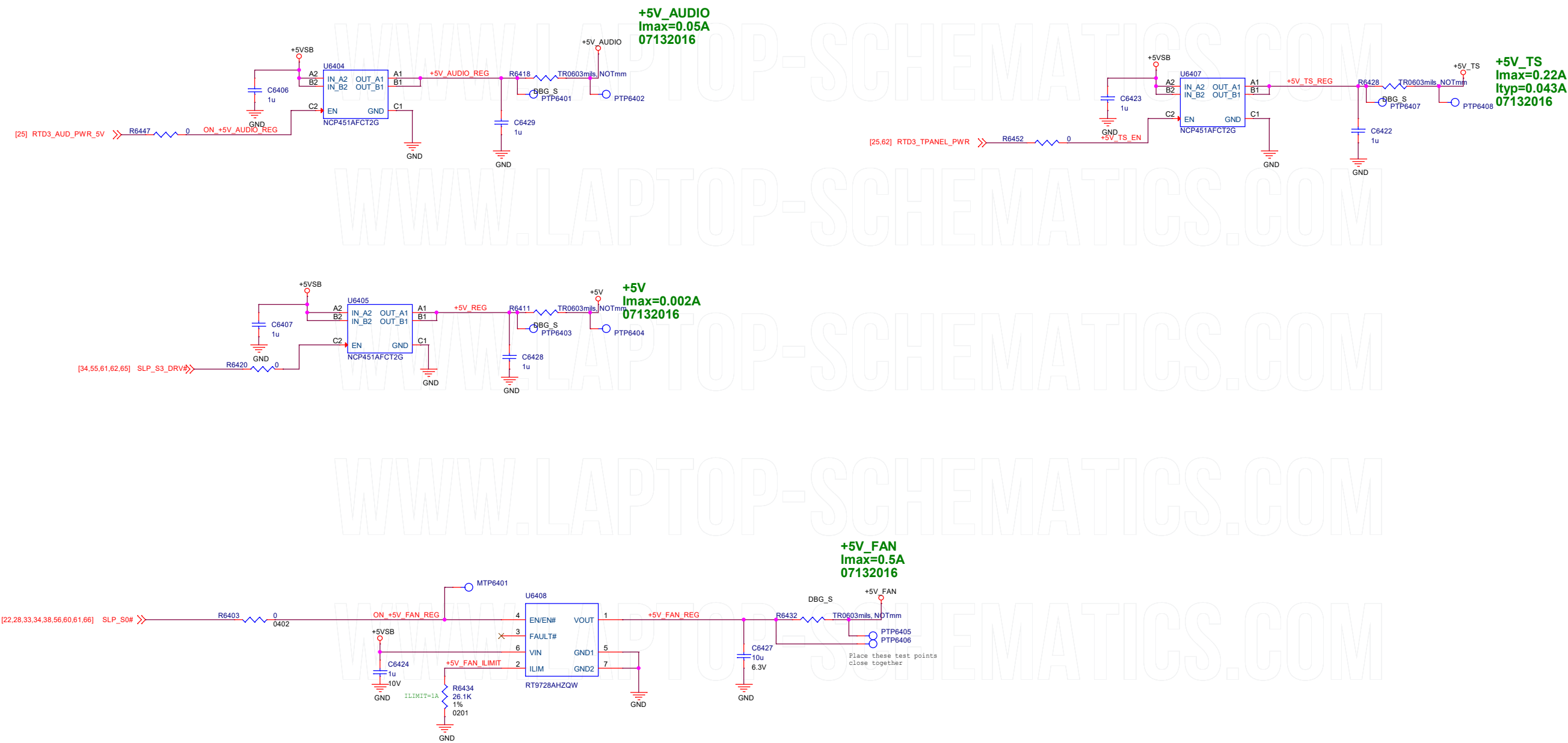


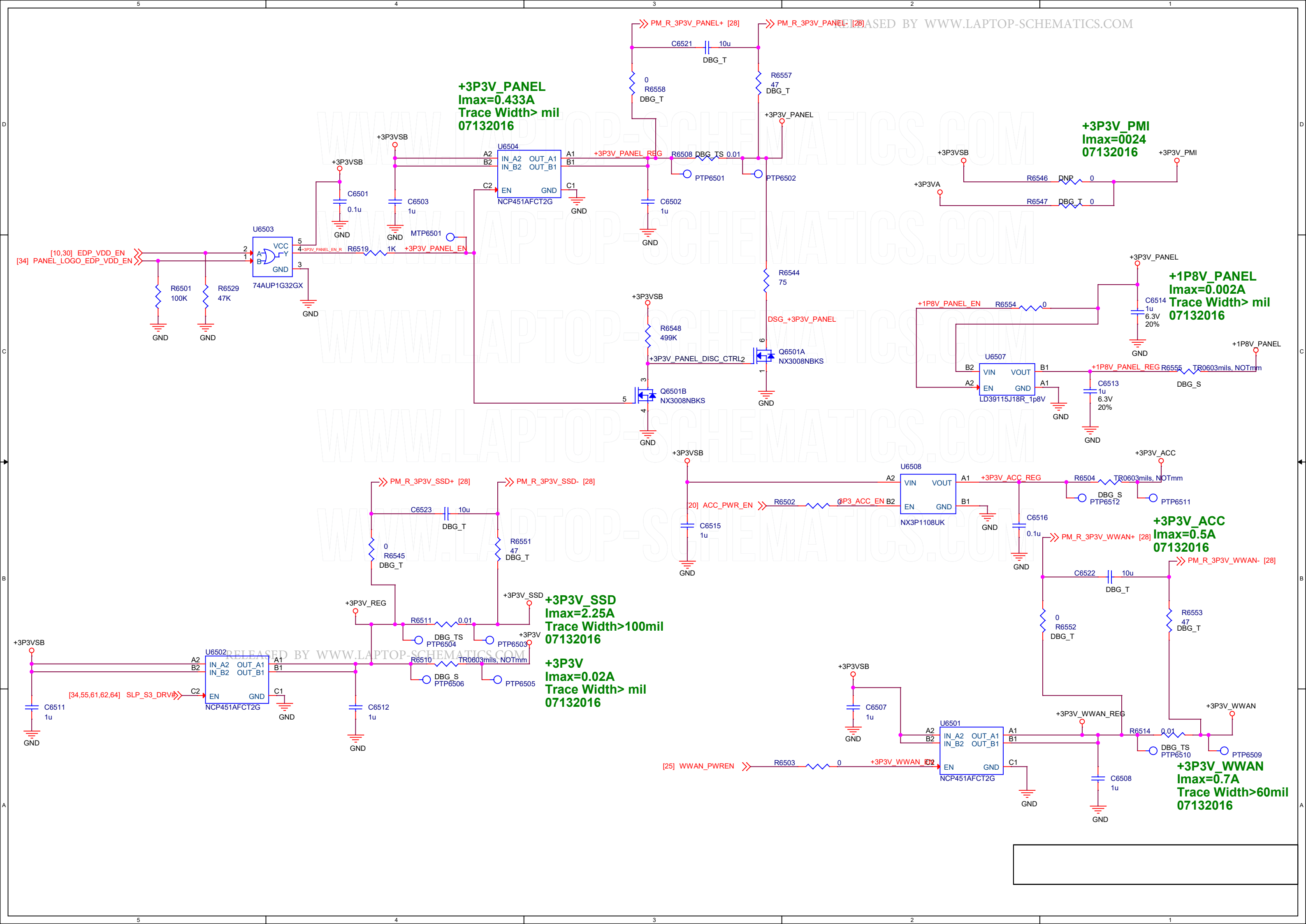


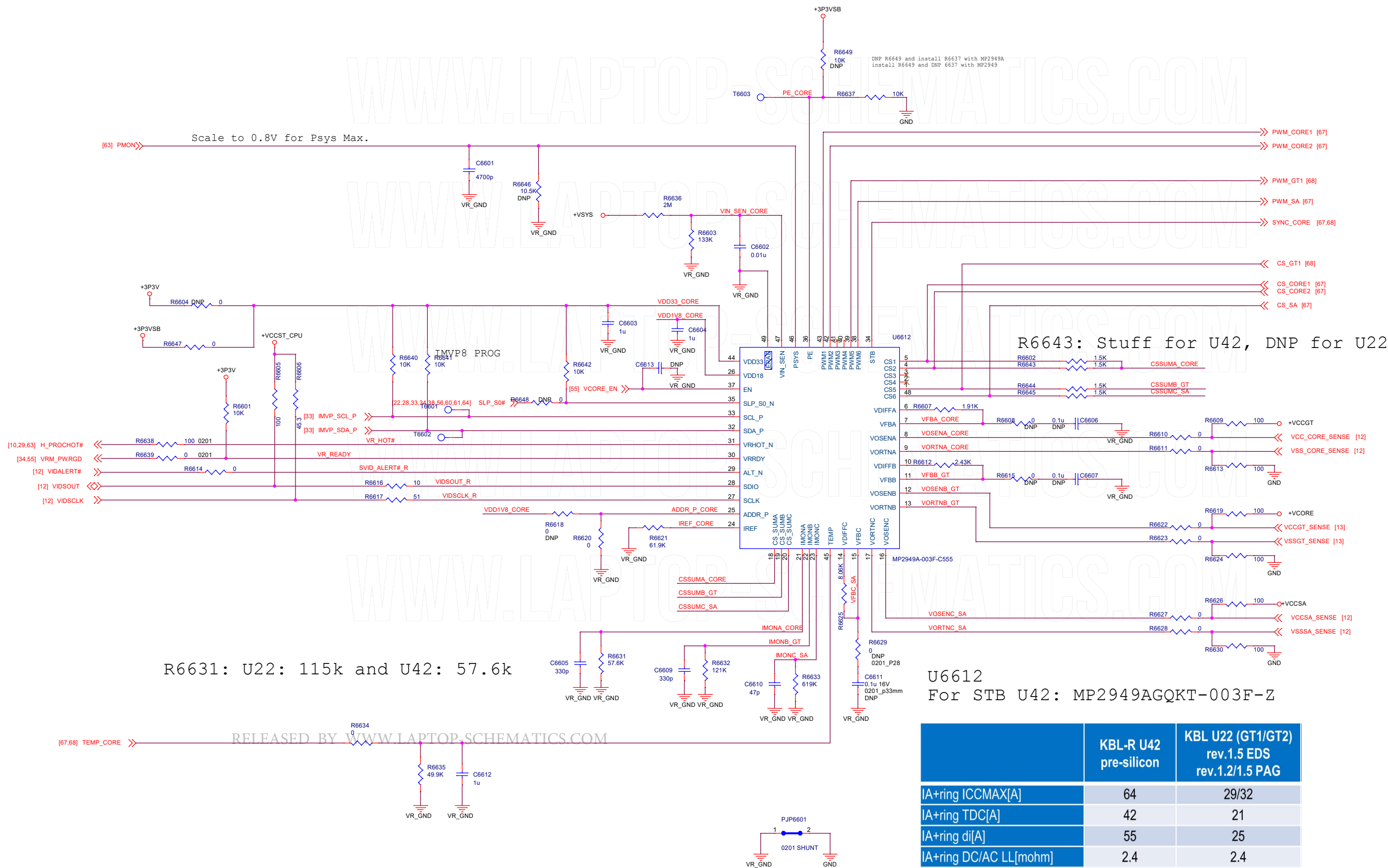












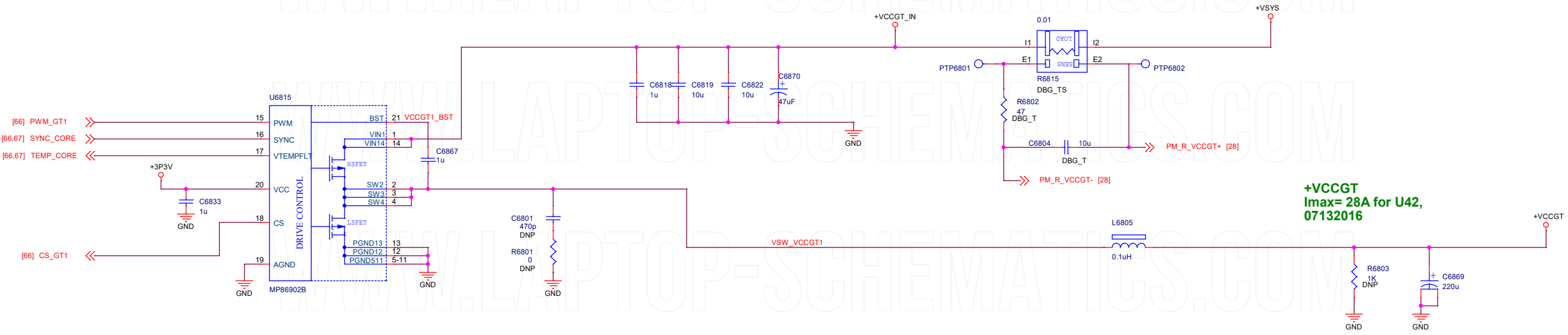
R6631: U22: 115k and U42: 57.6k

U6612  
For STB U42: MP2949AGQKT-003F-Z

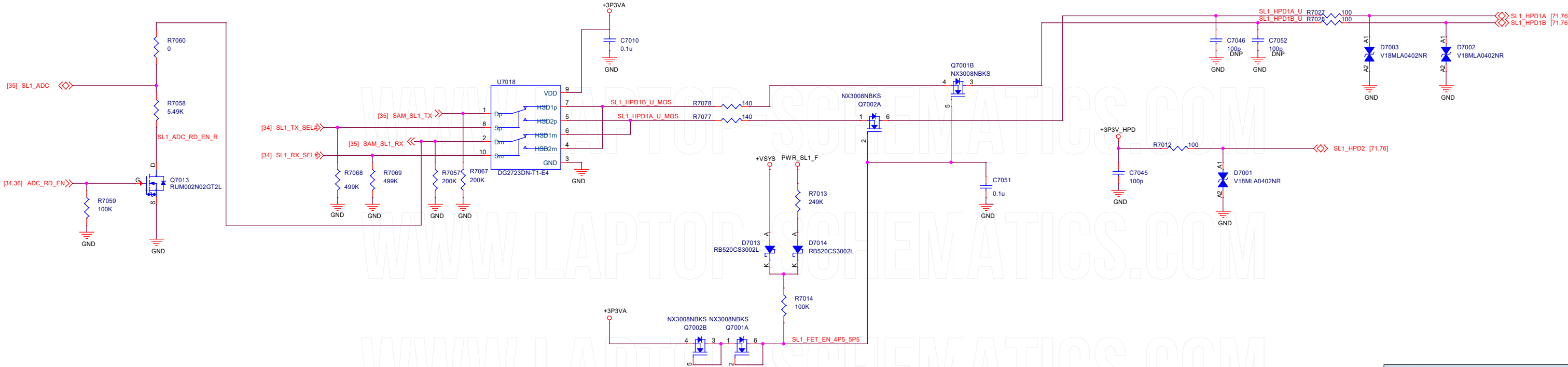
	KBL-R U42 pre-silicon	KBL U22 (GT1/GT2) rev.1.5 EDS rev.1.2/1.5 PAG
IA+ring ICCMAX[A]	64	29/32
IA+ring TDC[A]	42	21
IA+ring di[A]	55	25
IA+ring DC/AC LL[mohm]	2.4	2.4
GT ICCMAX S+US[A]	28	31
GT TDC[A]	12	18
GT di[A]	20	28
GT DC/AC LL[mohm]	3.1	3.1
SA ICCMAX[A]	5	4.5
SA DC/AC LL[mohm]	10.3	10.3
PL2 extreme[W]	51	29
PL4 extreme[W]	71	51







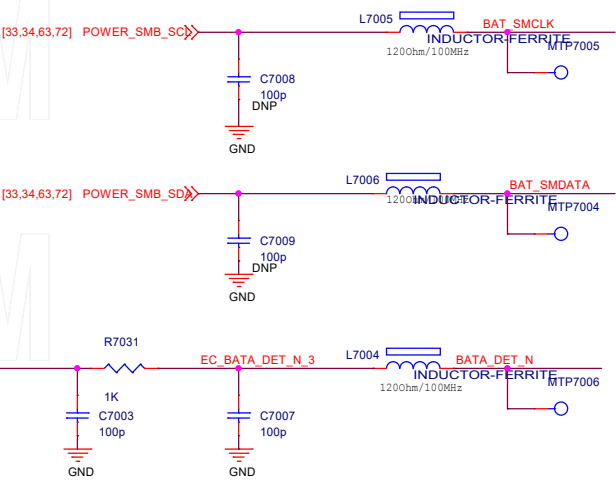




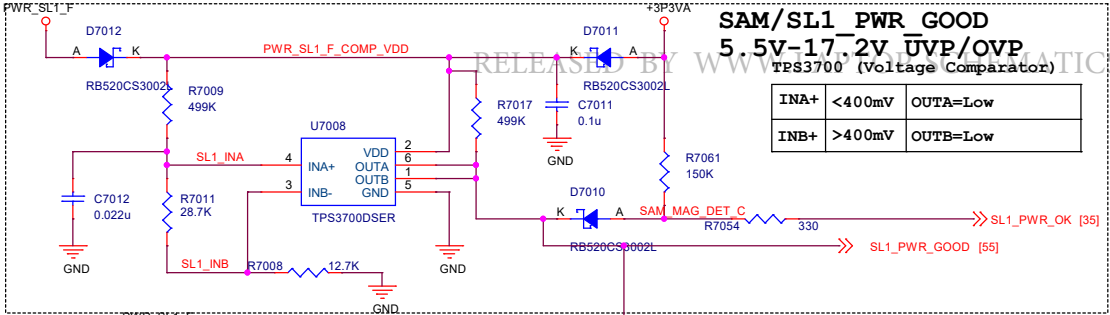
TRUTH TABLE		
S+ (PIN 8)	S- (PIN 10)	FUNCTION
X	0	D- = HSD1-
X	1	D- = HSD2-
0	X	D+ = HSD1+
1	X	D+ = HSD2+

Present State			Trigger	Output		
SL1_UART_TX	SL1_UART_RX	1W/2W Detect	Initial A/D read	SL1_UART_TX_SEL_N	SL1_UART_RX_SEL_N	SL Polarity
Low	Low	Detach	n/a	Low	Low	Detach
Low	High	1W	n/a	High	Low	Straight up
High	Low	1W	n/a	Low	High	Reversed
High	High	2W	Valid	Low	Low	Straight up
High	High	2W	Invalid	High	High	Reversed

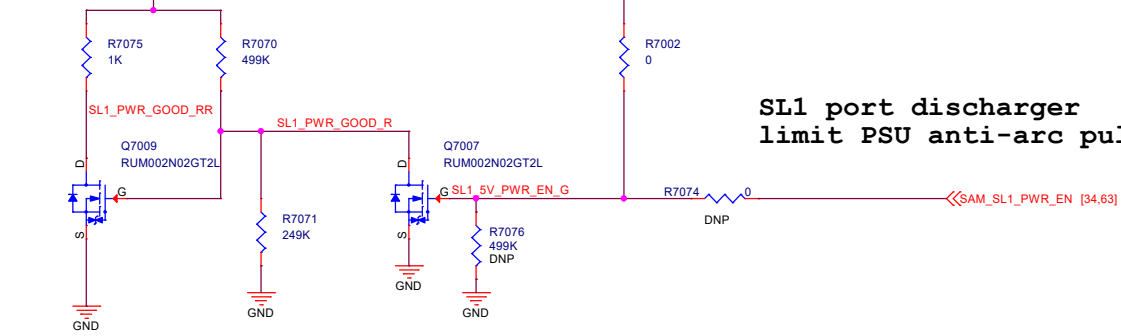
TPS3700 (Voltage Comparator)			
INA+	<400mV	OUTA=	Low
INB+	>400mV	OUTB=	Low



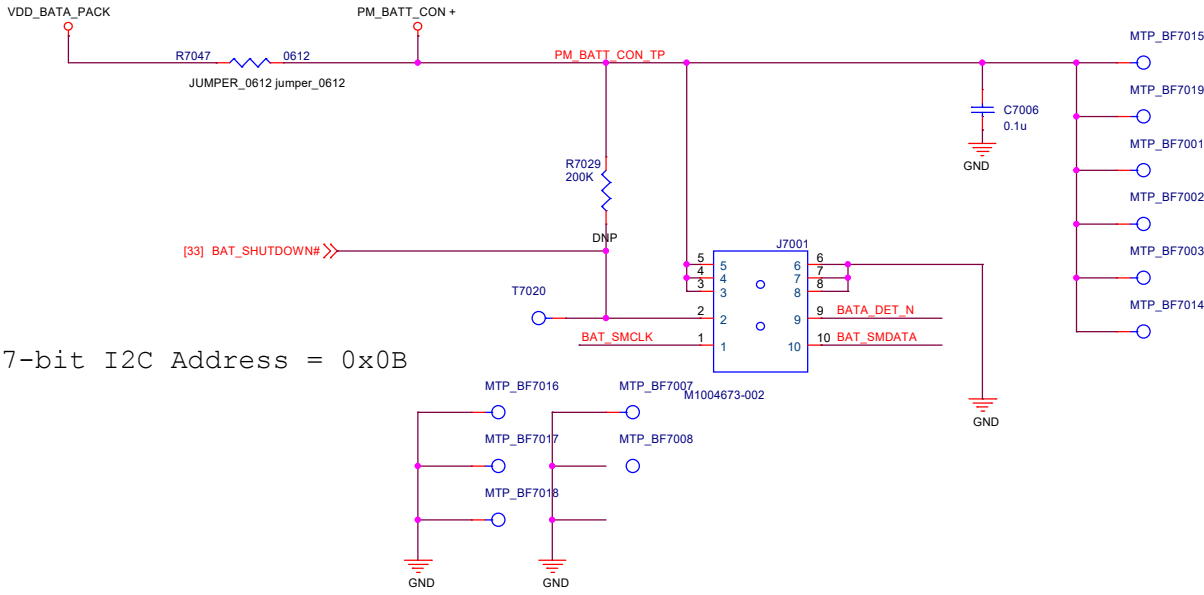
Base Battery lowest voltage



SL1 port discharger limit PSU anti-arc pulse voltage

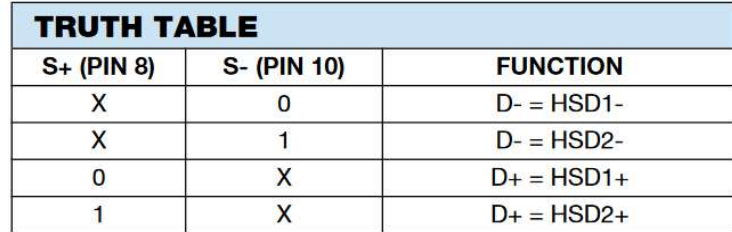
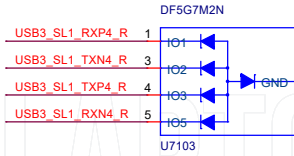
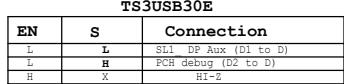


## 18W Battery Connector



7-bit I2C Address = 0x0B

The schematic diagram illustrates the DP12 to SL1 interface. It shows three differential signal pairs (DATA0, DATA1, DATA2) and their connections to SL1\_LANE1\_R, SL1\_LANE2P\_R, SL1\_LANE2N\_R, SL1\_LANE3N\_R, and SL1\_LANE3P\_R. The diagram includes components like resistors R7110, R7111, R7120, R7121, R7122, R7123, R7124, R7116, inductors L7102, L7103, L7104, and connectors DLP11TB800UL2L. A +3P3VA power source is also indicated.

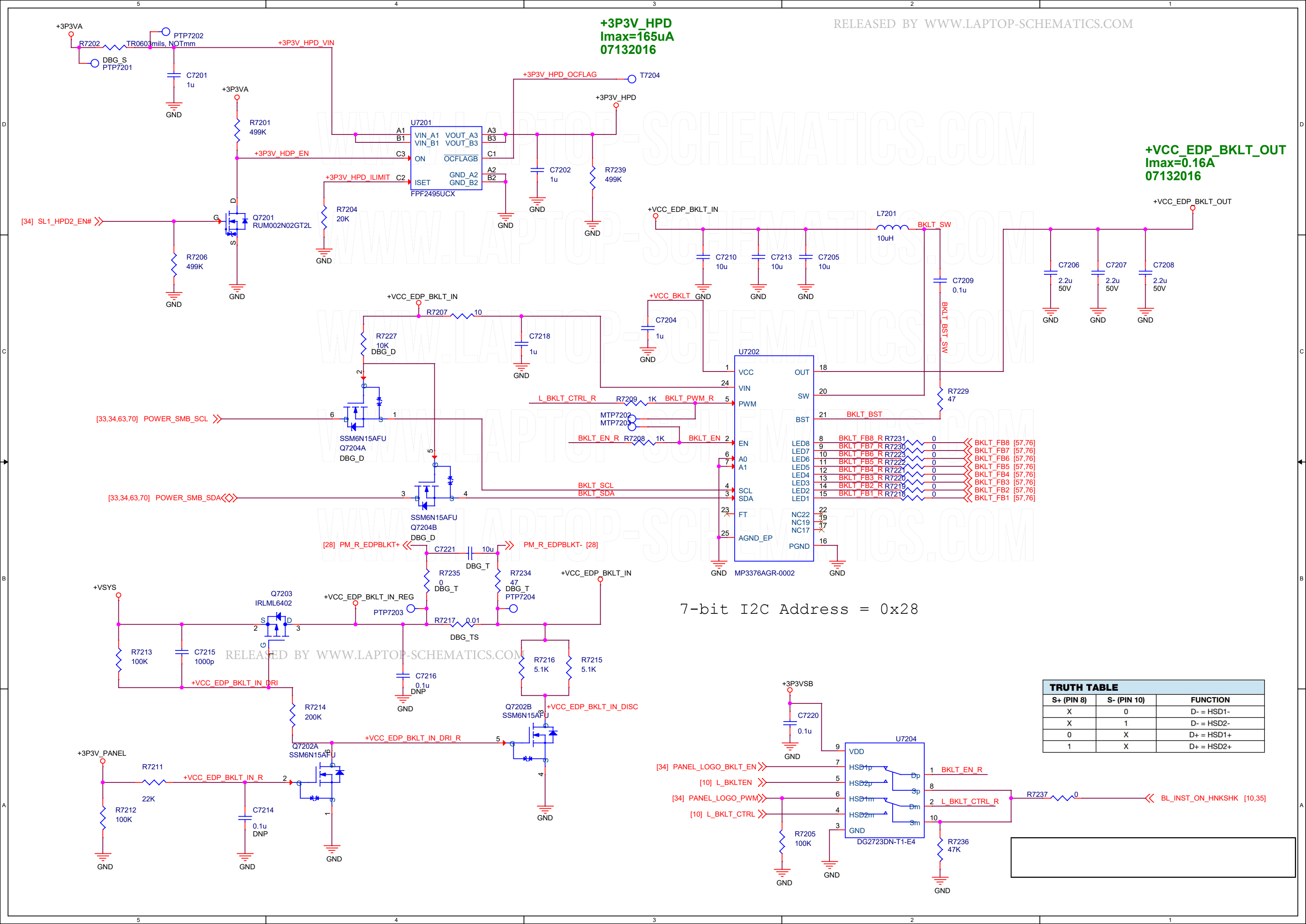
[illegible]

**+3P3V\_HPDP**  
**I<sub>max</sub>=165uA**  
**07132016**

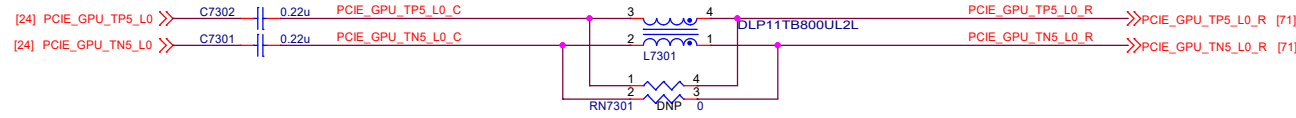
**+VCC\_EDP\_BKLT\_OUT**  
**I<sub>max</sub>=0.16A**  
**07132016**

7-bit I2C Address = 0x28

TRUTH TABLE		
S+ (PIN 8)	S- (PIN 10)	FUNCTION
X	0	D- = HSD1-
X	1	D- = HSD2-
0	X	D+ = HSD1+
1	X	D+ = HSD2+

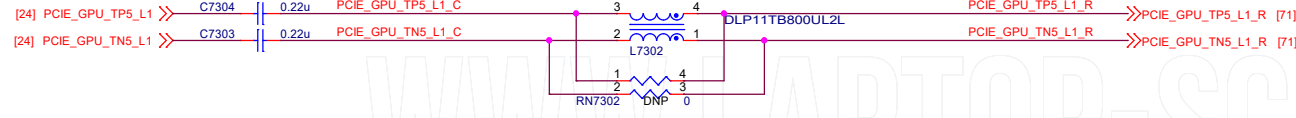
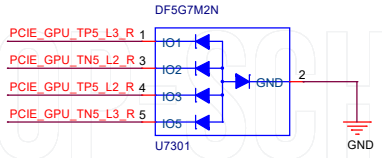






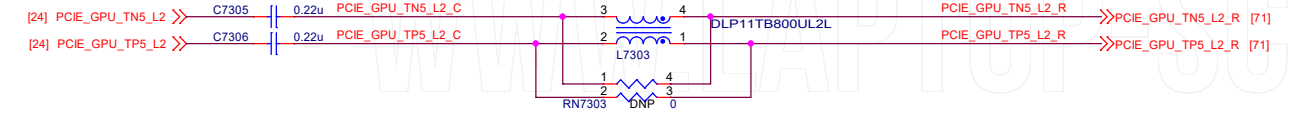
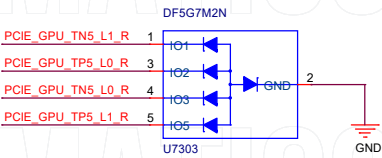
[24,71] PCIE\_GPU\_RN5\_L0 <<

[24,71] PCIE\_GPU\_RP5\_L0 <<



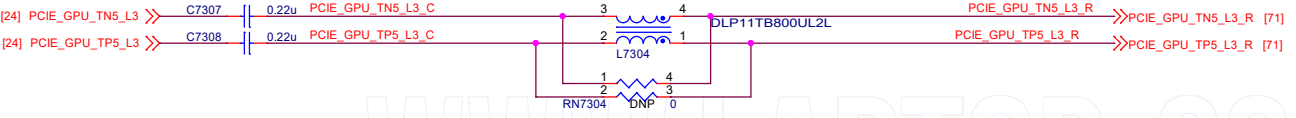
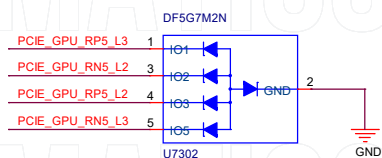
[24,71] PCIE\_GPU\_RN5\_L1 <<

[24,71] PCIE\_GPU\_RP5\_L1 <<



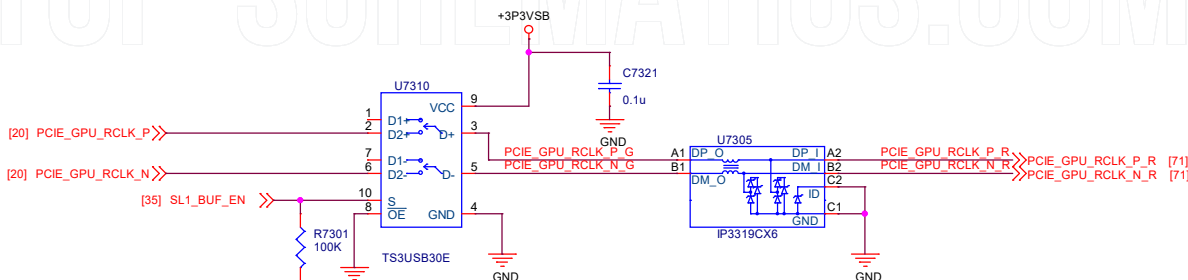
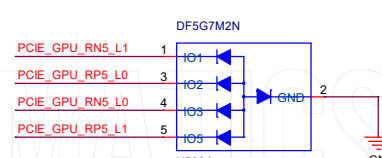
[24,71] PCIE\_GPU\_RN5\_L2 <<

[24,71] PCIE\_GPU\_RP5\_L2 <<



[24,71] PCIE\_GPU\_RP5\_L3 <<

[24,71] PCIE\_GPU\_RN5\_L3 <<



TS3USB30E		
EN	S	Connection
L	L	(D1 to D)
L	H	(D0 to D)
R	X	R1-2

